DSP56362EVMUM/AD
02/01
REV # 2.5

DSP56362EVM

User's Manual

Freescale Semiconductor, Inc.

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This manual is one of a set of three documents. You need the following manuals to have complete product information: Family Manual, User's Manual, and Technical Data.

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About This Manual

This manual describes the functionality and use of the DSP56362EVM (Evaluation Module). Motorola offers several different ROM software versions of the DSP56362 that are supported with this EVM. DSP56362 ROM versions are available to support technologies from third party licenses, such as Dolby Laboratories™, and DTS™.
Users can upgrade this EVM because critical components such as the DSP56362, MC68HC711, and EPROM are socketed. For information on other ROM versions, contact Motorola, or visit the website at:

http://mot-sps.com/ADC/audio_solutions.html

Organization

This book is organized into 6 sections:

- Overview
- Setup and Operation
- Component Datasheets
- Schematics
- Bill of Materials
- Running the Pass-through code

Suggested Reading

Additional reading that provides background for the information in this guide as well as general information about the Multimedia Architecture:

- IEC 958 Digital Audio Interface Standard
- DSP56362 User's Manual

Conventions

This document uses the following notational conventions:

- Messages displayed on screen and example code are presented in the `courier fixed-width font`.
- Information entered by users is shown in **bold** font.
- *File names*, *program names*, and *directories* are in italics.

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SECTION 1
OVERVIEW

1.1 INTRODUCTION

This section describes the basic features, hardware description and installation of the DSP56362EVM (Evaluation Module). The manual also describes the equipment and software required. Code samples and self-test code are provided on an accompanying software diskette. The schematic diagram and parts of the Evaluation Module are included in this manual. This is a generic hardware/software configuration. Upgrade kits are available for more specialized and advanced applications. Some upgrade kits require licensing agreements with other companies (DTS™, Dolby Digital™, etc.).The block diagram is shown in Figure1-1.

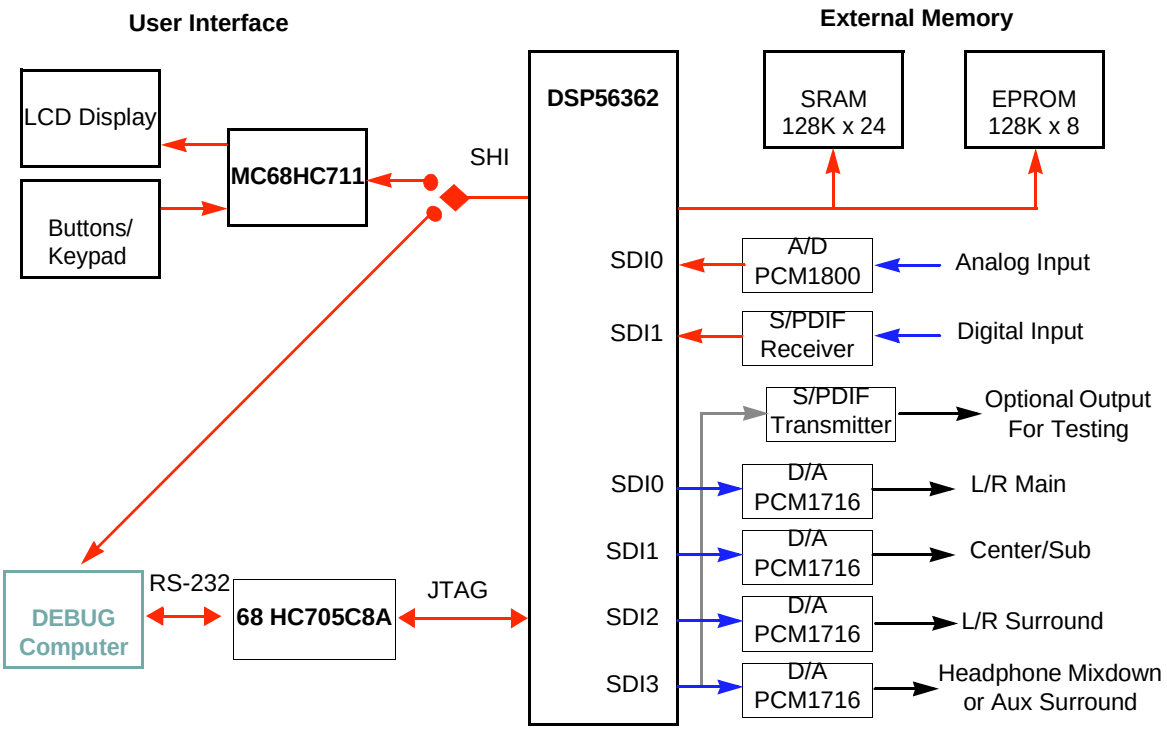

Figure 1-1 Figure1-1 Block diagram

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1.2 FEATURE DESCRIPTION

The DSP56362EVM is a low-cost platform for multichannel digital audio applications design, prototyping, and development. See Figure1-2.

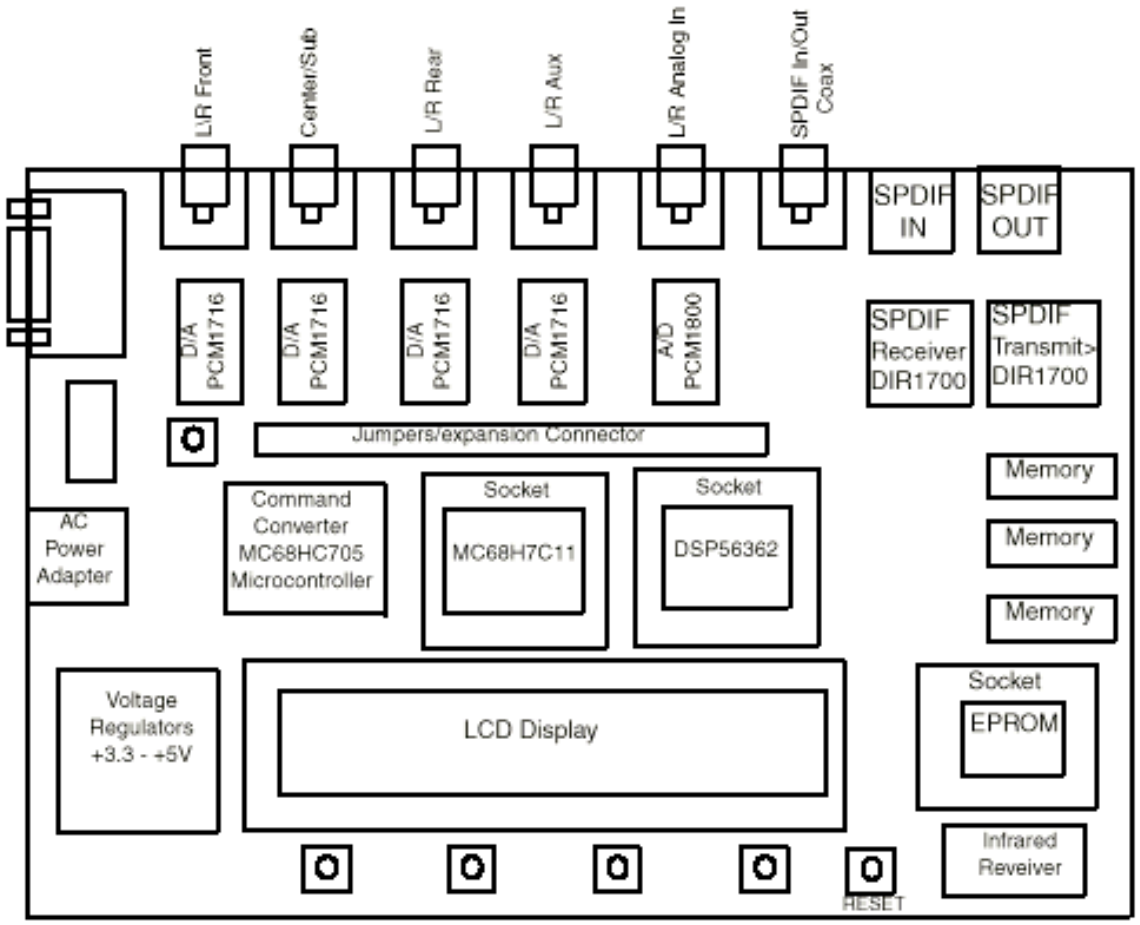

Figure 1-2 Consumer Audio Evaluation and Prototyping Platform

The fully assembled and tested circuit board contains the following.

- 24-bit DSP56362 Digital Signal Processor operating at 80-100MHz.
- 128k x 24-bits of external SRAM and 128k x 8-bits of EPROM.
- One 20-bit stereo Analog-to-Digital converter (ADC), four 24-bit stereo Digital-to-Analog converters (DACs).
- RCA jacks for all analog audio input and output connections.

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- Optical and transformer-isolated electrical S/PDIF stereo digital audio inputs and outputs.
- 50-pin expansion connector that provides capability for expansion and/or substitution of other input/output peripherals. This connector also simplifies interprocessor communication between other Motorola Evaluation Modules.
- Socketed MC68HC711E20 that allows users to substitute custom MC68HC711 code (allows connection to MC68HC11 emulation systems).
- 2 line x 20 character Liquid Crystal Display (LCD) and four soft switches for user interface.
- MC68HC705C8 microcontroller that performs RS-232-to-OnCE port command conversions.

1.3 HARDWARE DESCRIPTION

This section gives a brief summary of the Evaluation Module hardware supplied, and description of the hardware required to use the Evaluation Module.

1.3.1 EVALUATION MODULE HARDWARE

- Evaluation Module board
- Domain Technologies CD
- Debug - Evaluation Module manual is provided on the CD-DSP56362EVM User's Manual (this document)

1.3.2 USER SUPPLIED DEMONSTRATION HARDWARE

- An AC-3 or PCM bitstream source such as a Laserdisc, DAT, CD source, or VHS.
- An audio amplifier that can drive headphones or speakers as shown in Figure1-3.
- A 7.5- 9V 1 amp AC/DC power supply (7.5 volts is preferred).

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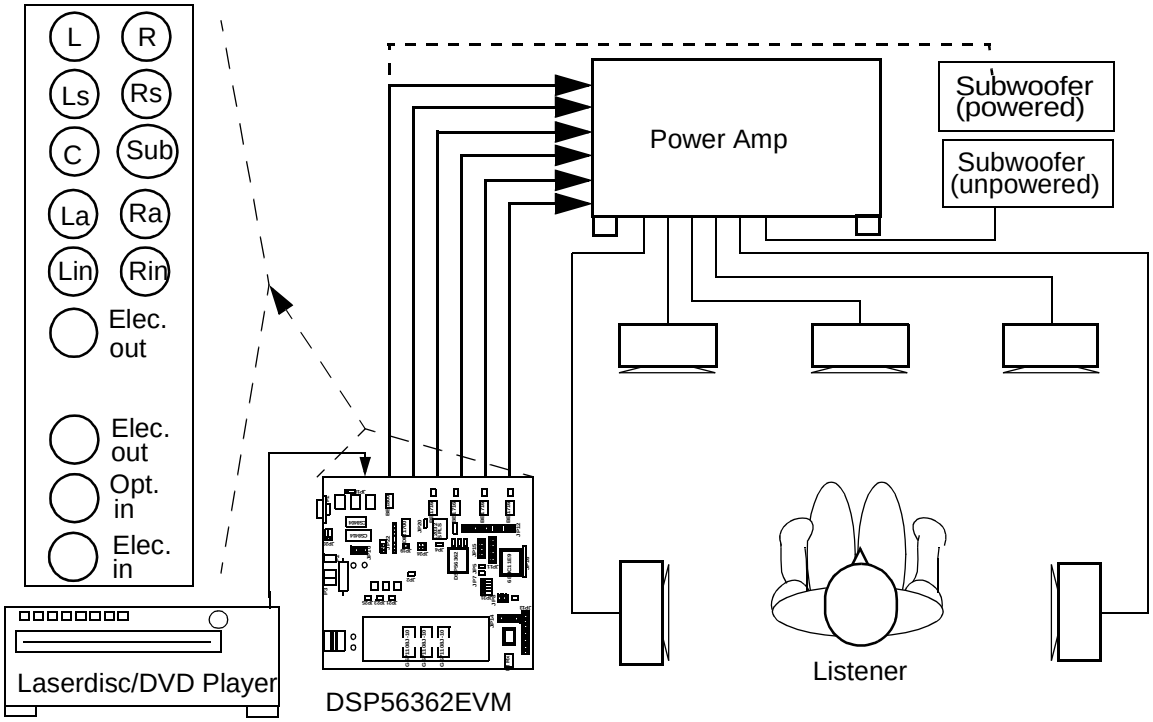

Figure 1-3 Demonstration Configuration

1.3.3 REQUIRED SOFTWARE DEVELOPMENT HARDWARE

- A personal computer with x386 or higher processor, minimum 2 Mbytes of memory, CD ROM driver, and a serial port that is capable of at least 19,200 bits-per-second data transfer rate.
- Windows 95/98 or NT operating system
- An RS-232 cable (DB9 male to DB9 female)

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1.4 INSTALLATION PROCEDURES

Installing the Evaluation Module requires four steps:

1. Preparing the board.
2. Connecting the board to the PC and power.
3. Installing the software on the PC.
4. Testing the installation.

1.4.1 HARDWARE CONNECTIONS

CAUTION

Because all electronic components are sensitive to the effects of electrostatic discharge (ESD) damage, use correct procedures when handling all components in this kit and inside the supporting PC. Use the following procedures to minimize the possibility of ESD damage.

- **Always handle all static-sensitive components in a protected area, preferably a lab with conductive (anti-static) flooring and bench surfaces.**
- **Always use grounded wrist straps when handling sensitive components.**
- **Never remove components from anti-static packaging until required for installation.**
- **Always transport sensitive components in anti-static packaging.**

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1.4.2 PC AND POWER CONNECTIONS

Figure1-4 shows the interconnection diagram for connecting the PC and the external power supply to the Evaluation Module board.

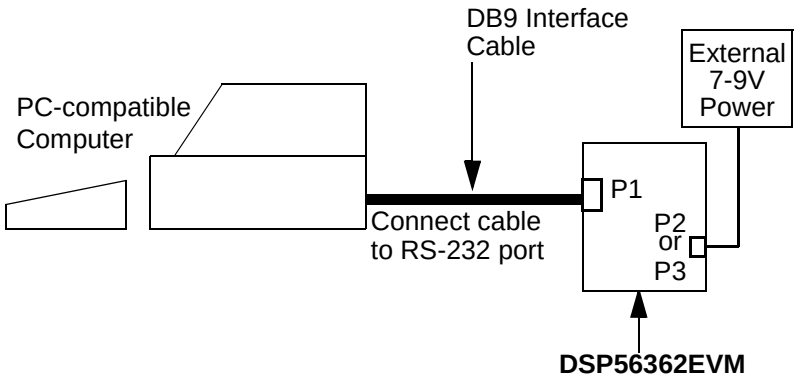

Figure 1-4 DSP56362EVM Cable Connections

1. Connect the DB9P interface cable to the RS-232 port connection on the PC, and P1 on the Evaluation Module board. This provides the connection to allow the PC to control the board function.
2. Apply 7.5-9V AC/DC 1amp power to the P2 or P3 connector on the Evaluation Module board.
3. The green Power LED will light when power is correctly applied.

1.4.3 SOFTWARE INSTALLATION

The Evaluation Module demonstration software consists of a Domain Technologies CD containing Windows™ style user interface debug software and demonstration/test code.Use the following steps to install the software:

1. Insert the Domain Technologies CD into the CD-ROM drive. Select and run the program **setup.exe.** Choose **DSP563xxEVM** from the menu.
2. Choose **Debug 56k** from the menu.
3. A Software License Agreement will appear. To install EVM563xx, you must accept this agreement. Click **yes**.
4. A new screen will appear. Fill in your **name** and **company**, then choose **NEXT**.

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5. Setup will install **EVM563xx** in **C:\Program Files\DomTech\EVM563xx,** then choose **NEXT.**
6. Setup will add program icons to the Program Folder. You may type a new folder name, or select one from the existing Folders list. Click **NEXT** to continue.
7. Setup has enough information to start copying the program files. Click **NEXT** to begin copying files.
8. The screen will clear and the Domain menu will appear. Click **EXIT**.

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SECTION 2

SETUP AND OPERATION

This section describes the setup options that you need to be familiar with. Jumpers on the Evaluation Module are provided to configure the board for various operations. The factory default jumpers are shown in Table 2-1. The locations of the headers for jumpers is shown in Figure 2-1.l

Table 2-1 Jumpers as Installed

Jumper	From	To	Jumper	From	To	Jumper	From	To
JP1	1	2	JP12	3	4	JP20	1	2
JP2	1	2		5	6	JP21	1	2
JP3	1	2		7	8	JP23	1	2
JP4	1	2		9	10	JP24	1	2
JP5	1	2		11	12	JP25	1	2
JP6	1	2		13	14	JP27	1	2
JP7	1	2		17	18	JP28	1	3
JP8	3	4		19	20		2	4
	7	8		21	22	JP31	2	3
				23	24		5	6
				25	26		8	9
				29	30		11	12
				31	32		14	15
				33	34	S6	1	
				35	36			
				43	44			
				45	46			
				47	48			

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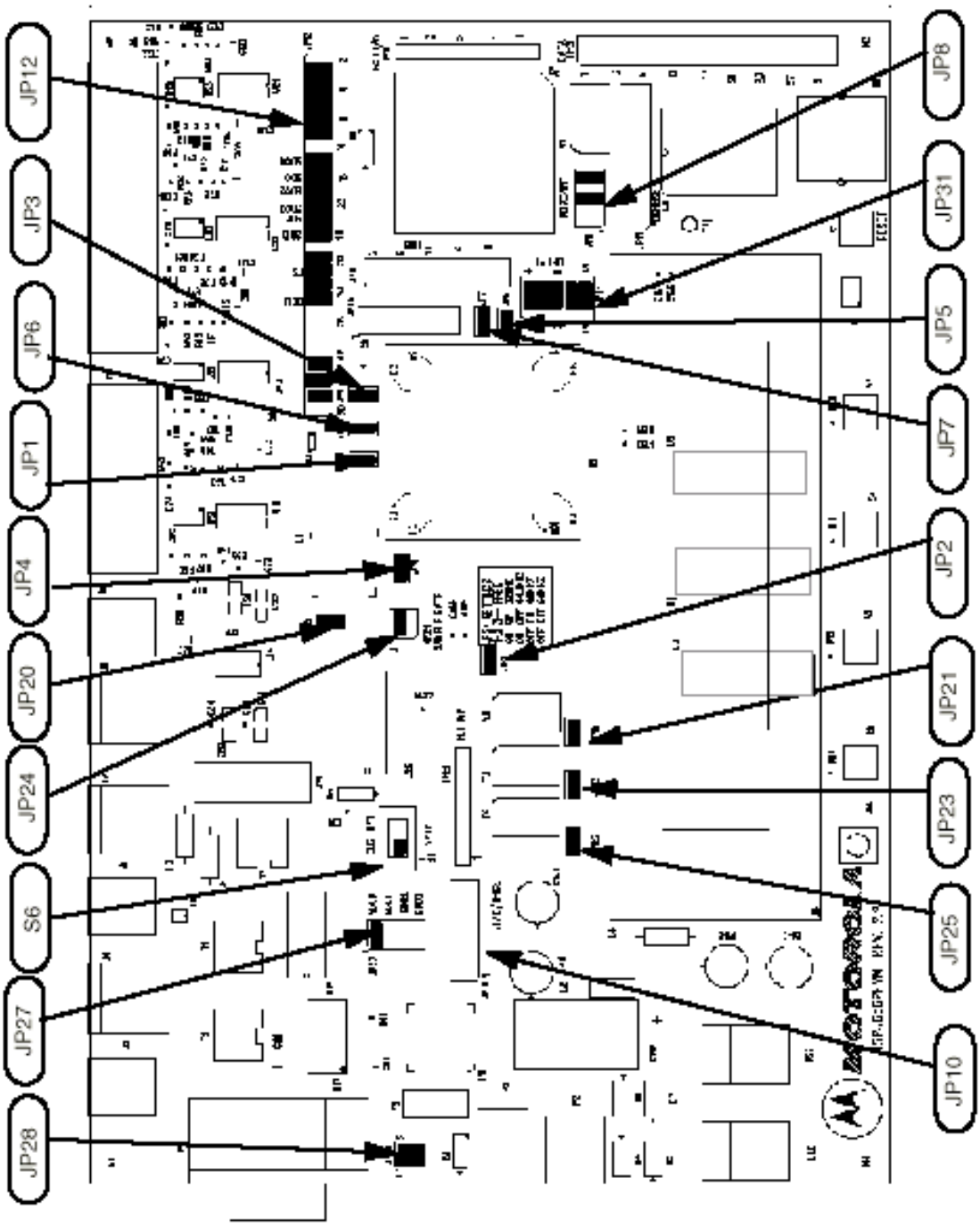

Figure 2-1 Default Jumper Locations Shown for Digital Input

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2.1 ANALOG I/O DESCRIPTION

The Evaluation Module has two analog input channels (Left and Right) and eight analog output channels.

1. Left
2. Right
3. Center
4. Subwoofer
5. Left Surround
6. Right Surround
7. Auxiliary channel 1
8. Auxiliary channel 2

Figure2-2 shows the analog input and output connectors.

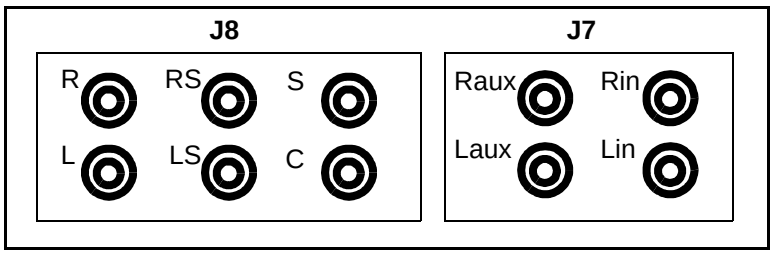

Figure 2-2 Analog I/O Connectors

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The A/D and D/A converters are clocked by the oscillators. Configure the header for analog input using the parameters as shown in the following table.

Table 2-2 Analog I/O Clocking Mode

JP 20 Pins 1-2	MODE
ON	CLOCKED BY S/PDIF RECEIVER (DIGITAL INPUT)
OFF	CLOCKED BY OSCILLATOR (ANALOG INPUT)

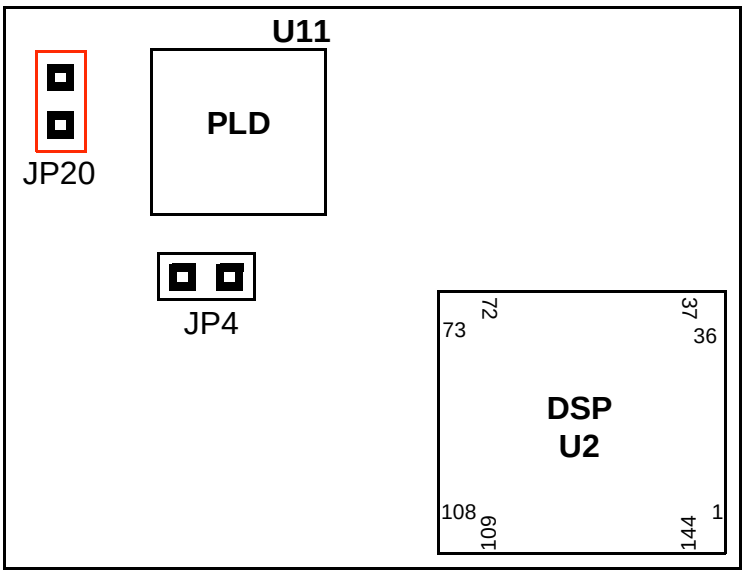

Figure 2-3 Input Clocking Mode Header PLD

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2.1.1 A/D CONVERTER DESCRIPTION

The system clock 256FS_CLK is input to the A/D and varies according to the selected oscillator which should be chosen according to the desired input sampling rate. Select the desired sampling rate by placing a jumper on the following header.

Table 2-3 A/D Sampling Rate Select

Sampling Frequency	JP24	
	Pins 1-2	Pins 3-4
32 KHZ	On	On
44.1 KHZ	On	Off
48 KHZ	Off	On
96 KHZ	Off	Off
Note: If U26 is populated with part number CS8412, the maximum sampling rate will be 48 KHZ.		

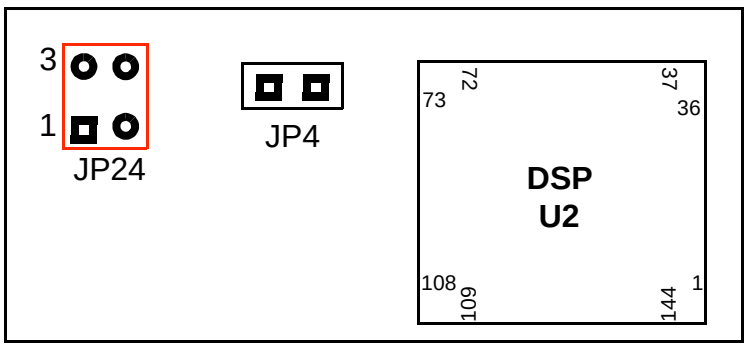

Figure 2-4 JP24, A/D Sampling Rate Select Header

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The receive and transmit serial clocks SCKR/SCKT operate synchronously and are derived from the PLD as BIT_CLK. The receive and transmit frame syncs FSR/FST also operate synchronously and are derived from the PLD as FS_CLK. These signals are derived from the PLD which divides the 256FS_CLK by 256 and by 4 to generate FS_CLK and BIT_CLK, respectively. The table below shows the clock relationships.

Table 2-4 System, Frame Sync and Serial Clocks

256FS_CLK	FS_CLK	BIT_CLK
8.192 MHZ	32 KHZ	2.048 MHZ
11.2896 MHZ	44.1 KHZ	2.8224 MHZ
12.288 MHZ	48 KHZ	3.072 MHZ
24.576 MHZ	96 KHZ	6.144 MHZ

2.1.1.1 Serial Data Input

The A/D converter sends audio data to the DSP on the serial data input SDI0.

2.1.1.2 A/D Converter Reset

The A/D converter is reset by asserting the RESET signal of the DSP.

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2.1.2 D/A CONVERTERS

The system clock 256FS_CLK is input to the D/As and varies according to the selected oscillator that corresponds to the input's sampling rate as described in Table 2-3. The four D/A converters operate in the slave mode so that the serial clock BIT_CLK and frame sync FS_CLK are inputs to the D/A converters.

2.1.2.1 Software Mode

The D/A converters operate in the software mode allowing for user control of the following functions:

- Input audio data format
- De-emphasis control
- Soft mute control
- Attenuation control
- Output phase selection
- DAC operation control

The default D/A converter settings are shown in the following table.

Table 2-5 DAC Default Settings

DESCRIPTION	DEFAULT
Audio data format	24-bit I^2S
Left channel attenuation	0 dB
Right channel attenuation	0 dB
Soft mute	OFF
De-emphasis	OFF
DAC operation	ON
Zero detect mute	OFF
Output analog signal phase	Normal
Attenuation control	Individual channel
L/R polarity	Left low/Right high

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The MC68HC711 microcontroller performs D/A converter initialization. DSP control of the D/A converters requires custom software. Refer to the Burr-Brown PCM1716E datasheet for detailed information on initializing the D/A converters. Table 2-6 describes the software mode control settings.

Table 2-6 D/A Software Mode Control

JP31		SELECT
CONTROL BY DSP	CONTROL BY PLD	
1-2	2-3	DA0 - L/R
4-5	5-6	DA1 - LS/RS
7-8	8-9	DA2 - C/S
10-11	11-12	DA3 - AUX L/R
13-14	14-15	ML

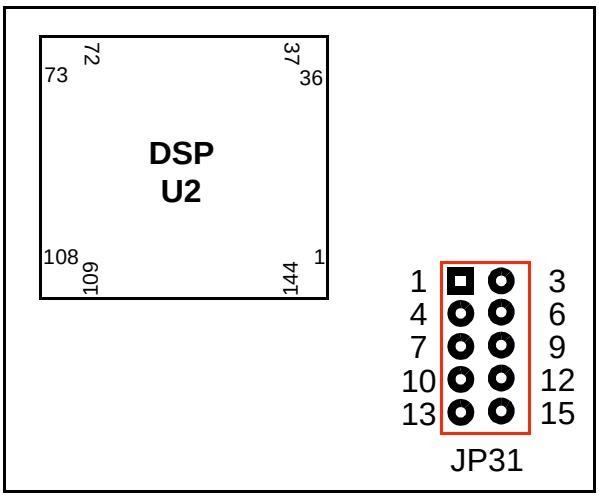

Figure 2-5 D/A Control Header

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2.1.2.2 Serial Data Outputs

The D/A converters receive audio data from the DSP on the following serial data outputs:

Table 2-7 D/A Serial Data Outputs

D/A	SDOx
L/R	SDO0
LS/RS	SDO1
C/S	SDO2
AUX L/R	SDO3

2.1.2.3 D/A Converter Reset

Asserting the DSP RESET signal, resets the D/A converters.

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2.1.3 ANALOG I/O BLOCK DIAGRAM

The following figure shows the functional block diagram of the analog I/O circuitry:

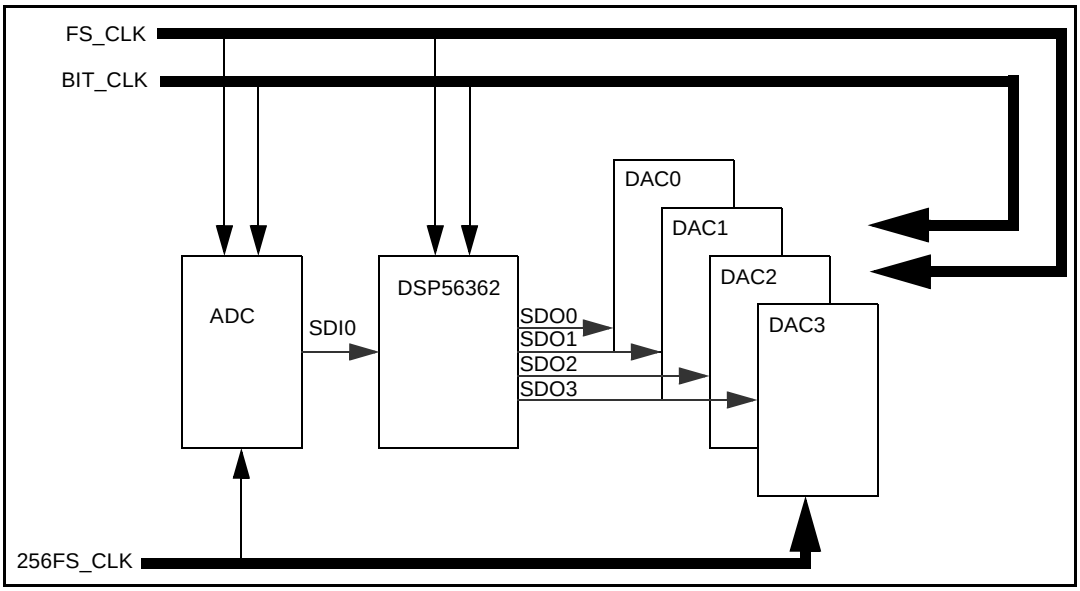

Figure 2-6 Analog I/O Block Diagram

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2.2 DIGITAL I/O

The Evaluation Module has coaxial and optical inputs, two coaxial and optical outputs, and it supports digital coaxial I/Os, and optical I/Os. The primary set of digital outputs are connected to the DSP Digital Audio Transmitter (DAX). The secondary set of digital outputs are connected to the S/PDIF transmitter. Figure 2-7 shows the digital input and output connector configuration.

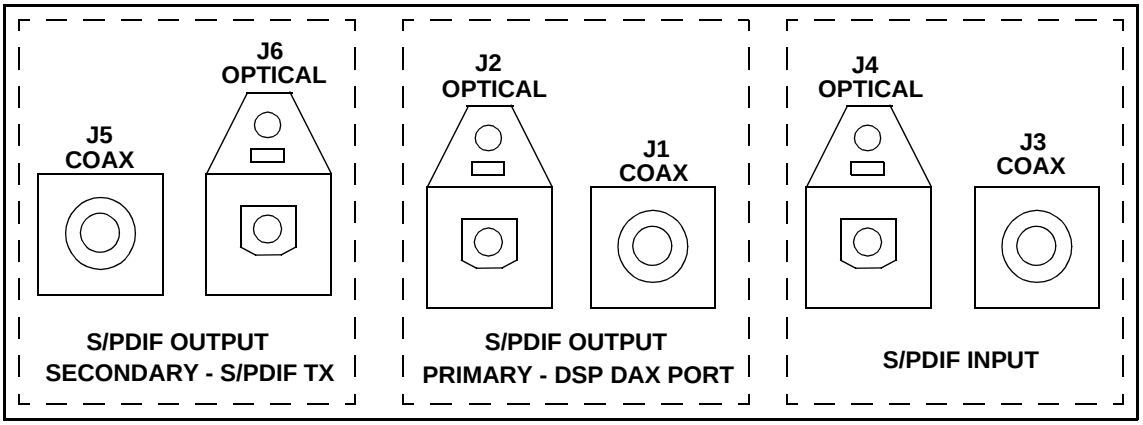

Figure 2-7 Digital I/O Connectors

Configure the JP20 header for digital input. Refer to Figure 2-1 and Figure 2-7.

Table 2-8 Digital I/O Clocking Mode

JP20 PINS 1-2	MODE
ON	CLOCKED BY S/PDIF RECEIVER (DIGITAL INPUT)
OFF	CLOCKED BY OSCILLATOR (ANALOG INPUT)

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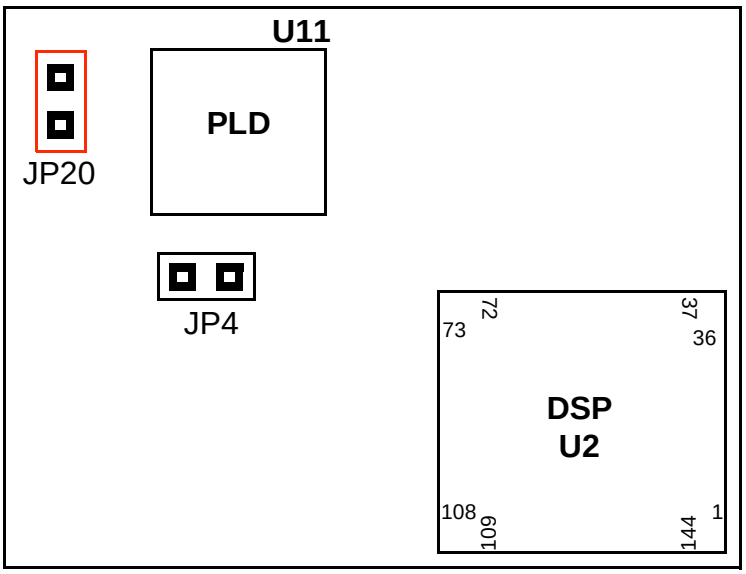

Figure 2-8 Input Clocking Mode Header

2.2.1 S/PDIF RECEIVER

The S/PDIF receiver recovers audio data and low jitter clocks from a digital audio transmission line. The generated clocks are the serial clock (BIT_CLK), frame sync (FS_CLK), and system clock (256FS_CLK). The S/PDIF receiver takes either coaxial or optical input. Selection is made by the position of S6 as follows:

Table 2-9 S/PDIF Receiver Select

S/PDIF INPUT	S6	Switch Position
COAXIAL	1	ELC
OPTICAL	2	OPT

The S/PDIF receiver sends audio data to the DSP on the serial data input SDI1.

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2.2.2 DIGITAL AUDIO TRANSMITTER

The Digital Audio Transmitter (DAX) outputs digital audio data in the AES/EBU, CP-340, and IEC958 formats. The DAX port connects to both coaxial and optical output connectors while the DAX clock input line (ACI) can be connected to an external clock source. This clock source must be 256fs, 384fs, or 512fs. The DSP transmits audio and non-audio data on the ADO pin.

2.2.3 S/PDIF TRANSMITTER

The S/PDIF transmitter operates in the consumer mode. The master clock 128FS_CLK varies according to the input sampling rate:

Table 2-10 S/PDIF Transmitter System Clock

SAMPLING FREQUENCY	128FS_CLK	FS_CLK	BIT_CLK
32KHZ	4.096MHZ	32KHZ	2.048MHZ
44.1KHZ	5.6448MHZ	44.1KHZ	2.8224MHZ
48KHZ	6.144MHZ	48KHZ	3.072MHZ

I^2S is the audio data format utilized on the DSP56362EVM.

The S/PDIF transmitter receives data from the DSP on the serial data output SDOx line. The SDOx is configured by placing a jumper on the JP27 header as shown below:

Table 2-11 S/PDIF Transmitter Serial Data Output

SDOx	JP27
SDO0	1-2
SDO1	3-4
SDO2	5-6
SDO3	7-8

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2.2.4 DIGITAL I/O BLOCK DIAGRAM

The functional block diagrams of the primary and secondary digital I/O circuits are shown in Figure 2-9 and Figure 2-10, respectively.

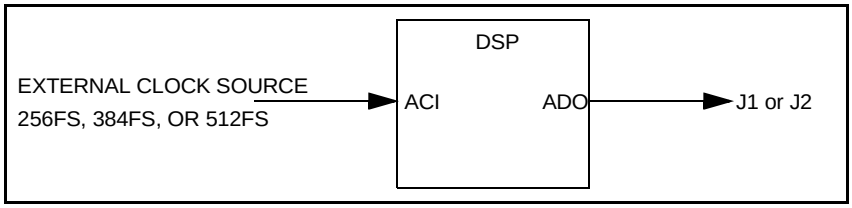

Figure 2-9 Primary Digital I/O Block Diagram

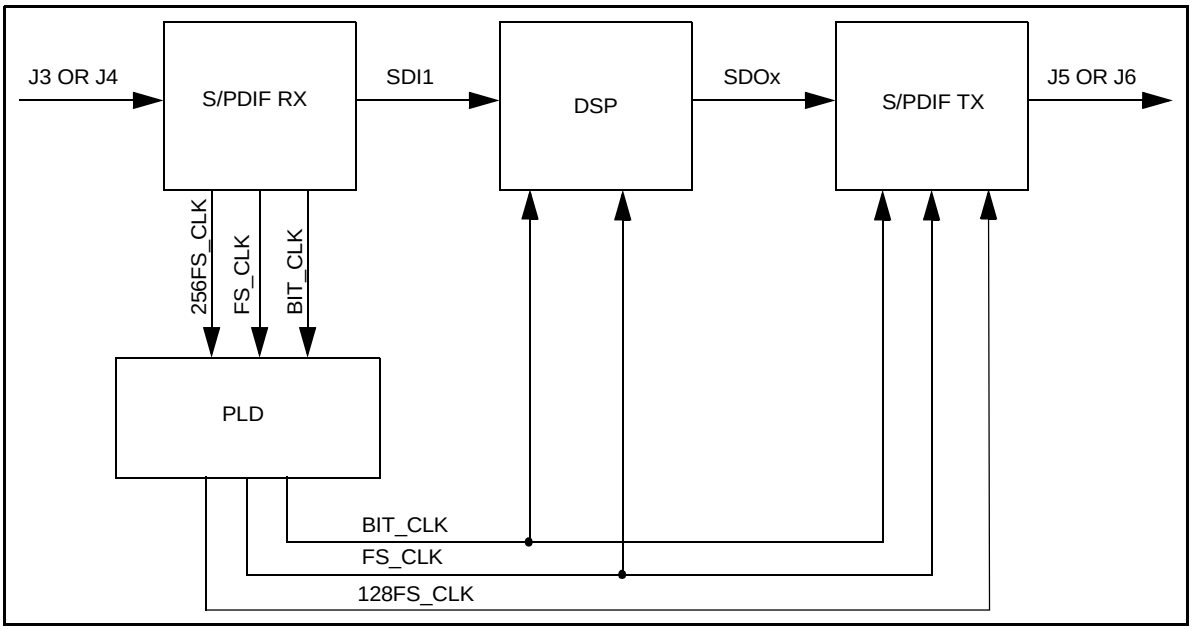

Figure 2-10 Secondary Digital I/O Block Diagram

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2.3 DSP CLOCK

The DSP clock is derived from the 8.192Mhz oscillator Y4. A voltage level converter is used because the DSP's EXTAL requires 3.3V operation. The $\overline{\text{PINIT}}$ signal is tied low, which disables the PLL when it resets. Because of this, the PLL's multiplication factor must be configured in user software. If the multiplication factor is not set, the DSP operating clock is 4.096Mhz (half of 8.192Mhz). Refer to Figure 2-15 for more information.

2.4 HOST MICROCONTROLLER INTERFACE

The MC68HC711E20 microcontroller communicates with the DSP using the Serial Host Interface (SHI) port in SPI mode. When SS is pulled low by the microcontroller, the microcontroller can write to the DSP. The MOSI and MISO lines pass control data through the DSP SHI in 24-bit mode. SCK is the SPI Shift Clock from the DSP.

The microcontroller also receives commands from the momentary push-button switches S2, S3, S4, or S5. The results of these commands are then displayed by a modular LCD panel with a 2 x 20 line character display. These commands control the settings of the executed software. The microcontroller also receives status information from the DSP.

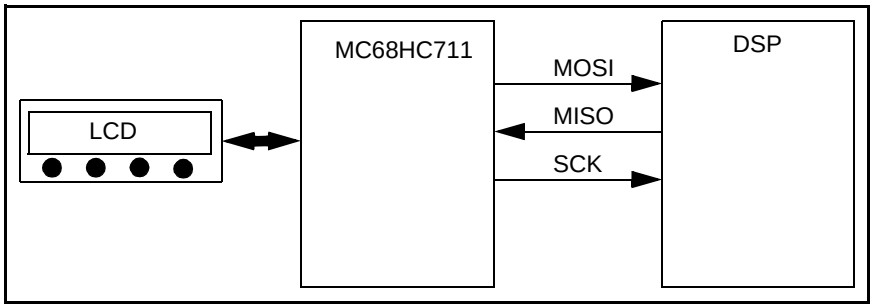

Figure 2-11 Host Microcontroller Block Diagram

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2.5 RS-232/MC68HC711 INTERFACE

Configure the header as shown in the following table, when using the RS-232 transceiver to communicate with the MC68HC711 microcontroller.

Table 2-12 RS232 Communication with MC68HC711

PINS	JP28
3-5	JUMPER
4-6	JUMPER

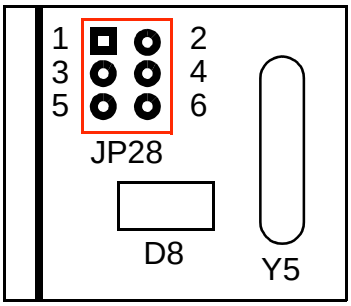

Figure 2-12 RS-232 Communication Select

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2.6 PLD FUNCTIONS

The PLD performs the following functions:

- Determines if S/PDIF or analog input is present.
- Performs clock division.
- Generates the DSP clock.
- Selects DACs for initialization.
- Inverts RESET signal for the HC08 microcontroller.

The PLD determines if the input to the DSP comes from the S/PDIF receiver or the A/D converter. If JP20 is jumpered (JUMP = logic 0) the PLD is notified that the input is from the S/PDIF receiver. In this case, the system clock, left/right clock, and bit clock that are generated by the S/PDIF receiver, are passed through the PLD as shown in Figure 2-13.

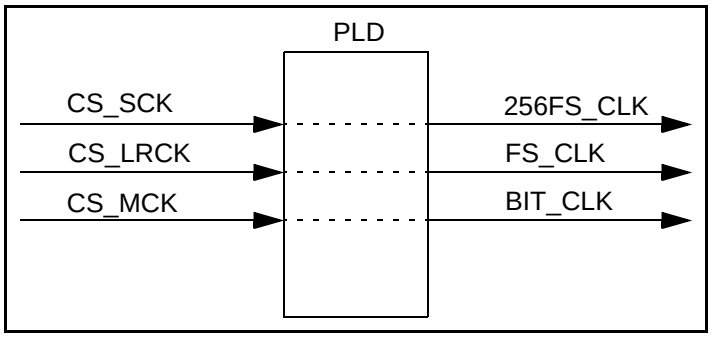

Figure 2-13 PLD Clock Outputs - S/PDIF

If JP20 is not jumpered (JUMP = logic 1) then the PLD assumes that the input is from the A/D converter. In this case, the system clock, left/right clock, and bit clock are generated from oscillators depending on the selected sampling rate on JP24. Figure 2-14 shows these sampling rates.

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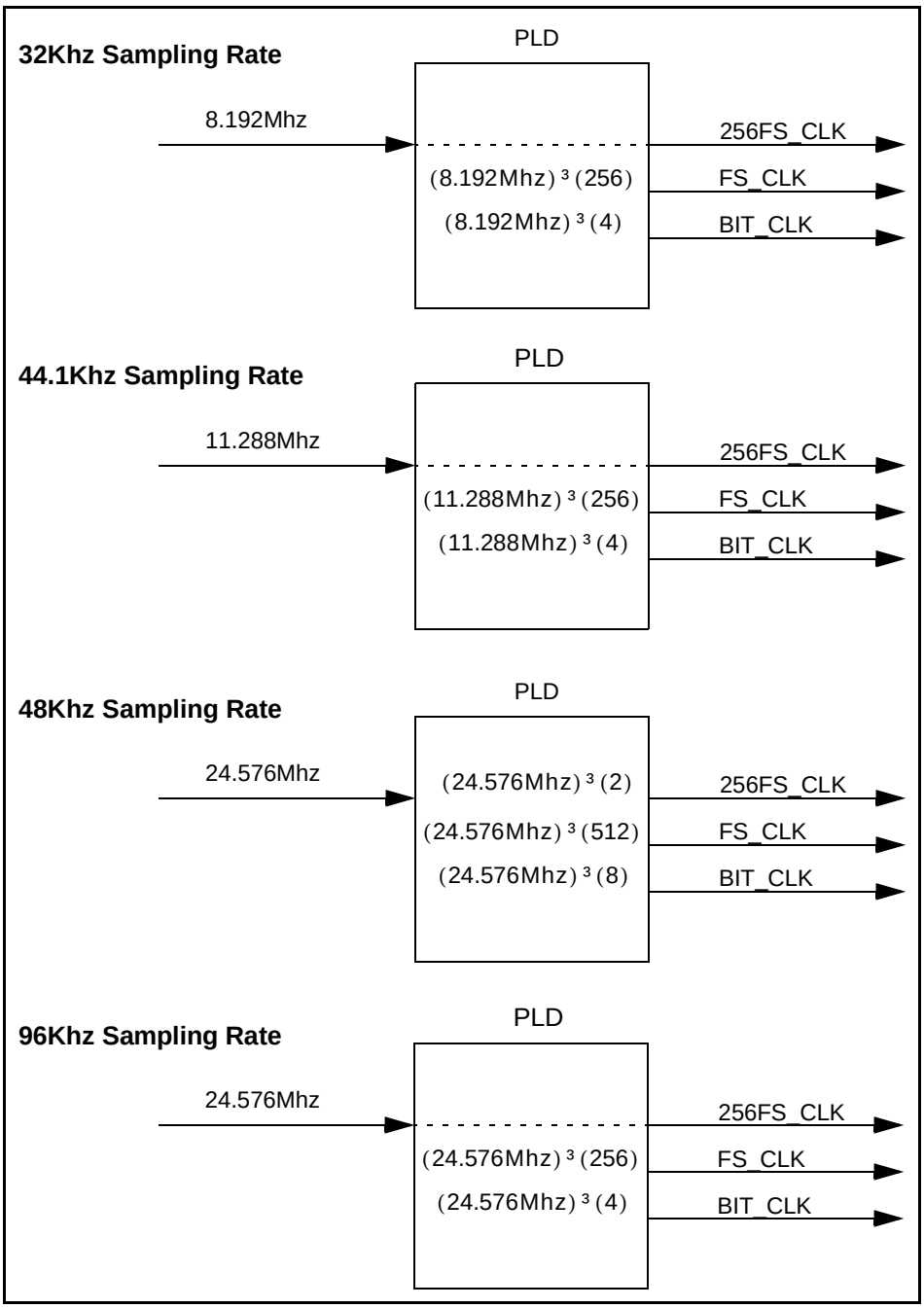

Figure 2-14 PLD Clock Outputs - A/D

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The default DSP clock source is 8.192 Mhz. If another clock source is required, modify the PLD equations and reprogram the PLD.

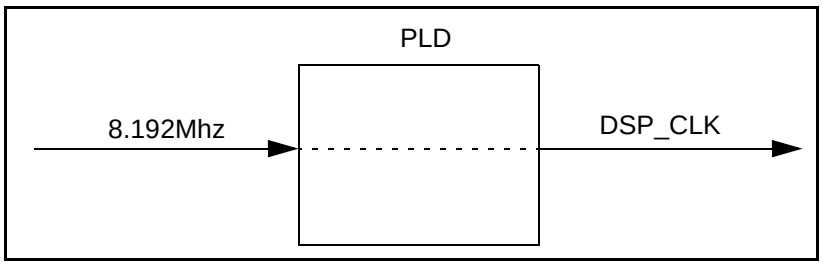

Figure 2-15 DSP Clock Source

All D/A converters are initialized after reset. For example, DA_SEL2 = logic 1, DA_SEL1 = logic 0, DA_SEL0 = logic 0. To individually initialize the D/A converters, modify the MC68HC711 microcontroller code to reflect the necessary changes.

Table 2-13 D/A Converter Select

D/A INITIALIZED	DA_SELx = 1	DA_SELx = 0
DA0	DA_SEL0	DA_SEL1 DA_SEL2
DA1	DA_SEL1	DA_SEL0 DA_SEL2
DA2	DA_SEL1 DA_SEL2	DA_SEL0
ALL DAs	DA_SEL2	DA_SEL0 DA_SEL1

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The PLD inverts the output from the RS-232 transceiver to the HC08 microcontroller as shown in the following figure.

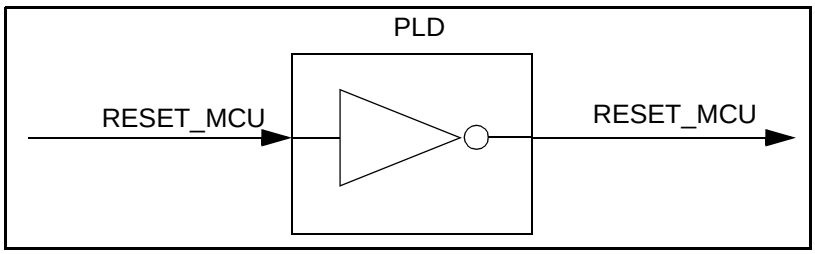

Figure 2-16 HC08 Reset

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2.7 OPERATING MODE SELECTION

DSP operating modes are selected by configuring JP8 as shown in Figure 2-17 and in the following table.

Table 2-14 DSP Operating Mode

MODE	DESCRIPTION	JP8			
		PINS 7-8 MODD	PINS 5-6 MODC	PINS 4-3 MODB	PINS 2-1 MODA
0	EXPANDED MODE	ON	ON	ON	ON
1	BOOTSTRAP FROM BYTE-WIDE MEMORY	ON	ON	ON	OFF
2	JUMP TO PROM STARTING ADDRESS	ON	ON	OFF	ON
5	BOOTSTRAP FROM SHI (SLAVE SPI MODE)	ON	OFF	ON	OFF
7	BOOTSTRAP FROM SHI (SLAVE I^2C MODE)	ON	OFF	OFF	OFF
8	EXPANDED MODE	OFF	ON	ON	ON
C	HI08 BOOTSTRAP IN ISA MODE	OFF	OFF	ON	ON
D	HI08 BOOTSTRAP IN MC68HC711 NON-MUX MODE	OFF	OFF	ON	OFF
E	HI08 BOOTSTRAP IN 8051 MUX BUS MODE	OFF	OFF	OFF	ON
F	HI08 BOOTSTRAP IN 68302 BUS MODE	OFF	OFF	OFF	OFF

Refer to the DSP56362 User's Manual for a detailed description of the operating modes.

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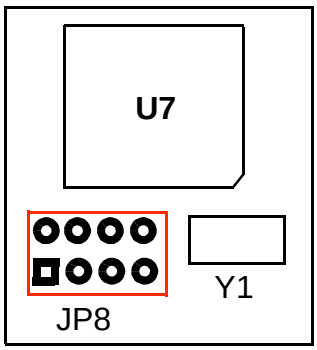

Figure 2-17 Operating Mode Jumper (JP8) Location

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2.8 EXPANSION PORT

The expansion port connector allows users to connect the DSPÆs SHI, ESAI, DAX and Timer ports to other input and output devices.

Table 2-15 Expansion Connector

JP12		SIGNAL	JP12		SIGNAL
EXTERNALSIDE	DSP SIDE		EXTERNALSIDE	DSP SIDE	
1	2	+3.3V	27	28	GND
3	4	MOSI	29	30	FST
5	6	MISO	31	32	FSR
7	8	SCK	33	34	SCKT
9	10	SS	35	36	SCKR
11	12	HREQ	37	38	HCKT
13	14	+5V	39	40	HCKR
15	16	SDO0	41	42	GND
17	18	SDO1	43	44	ADO
19	20	SDO2	45	46	ACI
21	22	SDO3	47	48	TIO0
23	24	SDI1	49	50	GND
25	26	SDI0			

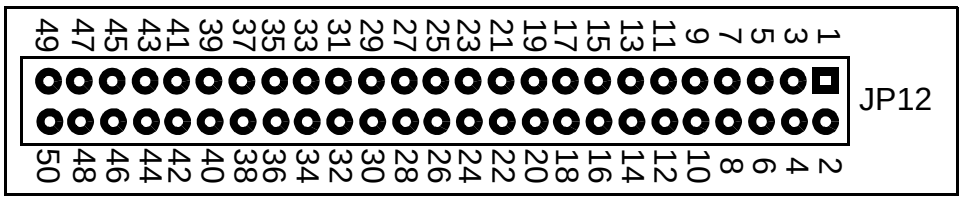

Figure 2-18 Expansion Connector

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2.9 ONCE PORT

The Evaluation Module has an on-chip emulation (OnCE™) connector that provides a means of interacting with the DSP and its peripherals non-intrusively. This allows users to examine registers, memory, or on-chip peripherals which facilitates hardware and/or software development. Perform debugging with the OnCE™ port in two ways.

1. A direct OnCE™ connection for use with an external command converter.
2. A serial RS-232/OnCE™ connection for use with the on-board command converter.

2.9.1 DIRECT ONCE CONNECTION

The OnCE connector allows an external command converter to communicate with the DSP. The following table specifies the OnCE signals. Refer to Figure 2-1 for location of JP10.

Table 2-16 OnCE Port Connector

JP10 PIN	SIGNAL	JP10 PIN	SIGNAL
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NO CONNECT	8	NO CONNECT
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V	12	NO CONNECT
13	$\overline{\text{DE}}$	14	$\overline{\text{TRST}}$

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2.9.2 RS-232/ONCE INTERFACE

The on-board command converter also allows debugging using the OnCE port. The RS-232/OnCE interface receives the serial data from the RS-232 transceiver and executes commands sent by the host computer. These commands can reset the DSP, put the DSP in debug mode, release the DSP from debug mode, read and write to the OnCE port, and read and write to the DSP itself. The RS-232 serial communication is performed in software on the MC68HC705 microcontroller. When using the RS-232 transceiver to communicate with the MC68HC705C8, configure the header as shown in the following table. Refer to Figure 2-1 and Figure 2-19 for header location.

Table 2-17 RS-232 Communications with MC68HC705

PINS	JP28
1-3	JUMPER
2-4	JUMPER

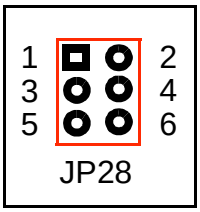

Figure 2-19 RS-232 Communication Select

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2.10 MEMORY

The Evaluation Module has glueless connection to external SRAM and EPROM. The following memory lines are connected to an expansion header. See Figure 2-20.

Table 2-18 Memory Line Settings

HEADER	PIN	SIGNAL	HEADER	PIN	SIGNAL	HEADER	PIN	SIGNAL
JP13	1	D0	JP14	1	A0	JP15	3	AA0
	2	D1		2	A1		5	AA1
	3	D2		3	A2		7	AA2
	4	D3		4	A3		9	AA3
	7	D4		5	A4		4	$\overline{BB}$
	8	D5		6	A5		6	$\overline{BG}$
	9	D6		7	A6		8	$\overline{BR}$
	10	D7		8	A7		10	$\overline{TA}$
	13	D8		9	A8		11	$\overline{RD}$
	14	D9		10	A9		12	$\overline{CAS}$
	15	D10		11	A10		13	$\overline{WR}$
	16	D11		12	A11			
	19	D12		13	A12			
	20	D13		14	A13			
	21	D14		15	A14			
	22	D15		16	A15			
	25	D16		17	A16			
	26	D17		18	A17			
	27	D18						
	28	D19						
	31	D20						
	32	D21						
	33	D22						
	34	D23						

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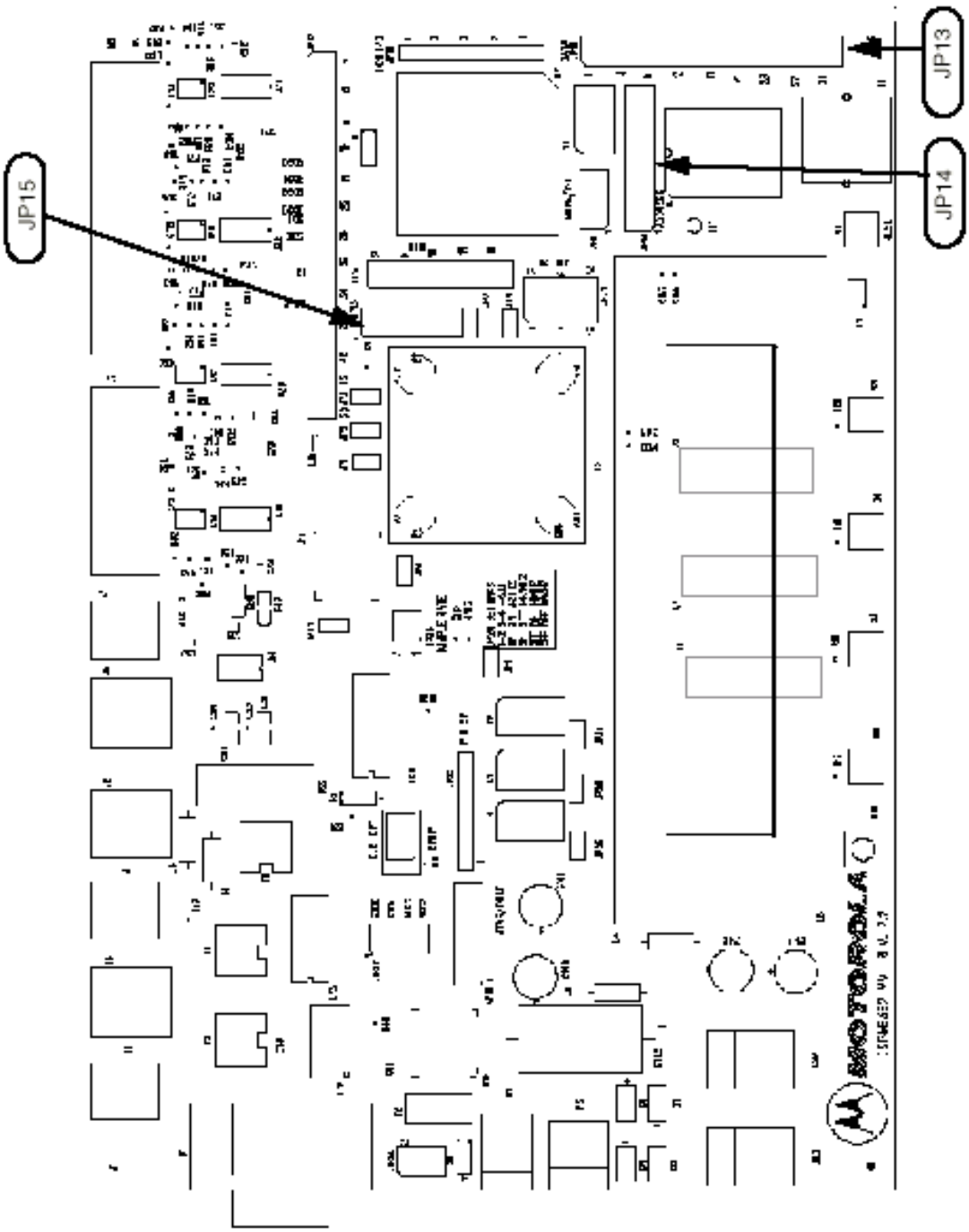

Figure 2-20 Memory Header Locations

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2.10.1 SRAM

The Evaluation Module has 128k x 24-bits of external asynchronous static RAM (SRAM). To keep the address stable during the entire bus cycle, insert a minimum of 1 wait state to the bus operation.

Select the SRAM by configuring the DSP's address attribute register to assert the AA2 line. The SRAM can be upgraded up to 512k x 24-bits. When using 512k x 24-bits of SRAM, the upper half of memory is accessible by controlling the address attribute line AA0. AA0 is connected to the memory's most significant address line.

2.10.2 EPROM

The Evaluation Module has 128k x 8-bits of EPROM. To keep the address stable during the entire bus cycle, insert a minimum of 1 wait state to the bus operation.

Select the EPROM by configuring the DSP's address attribute register to assert the AA1 line.

2.10.3 EXTERNAL MEMORY BLOCK DIAGRAM

The following figure shows the functional block diagram of the external memory interface.Memory data is accessible through the JP13-JP15 headers.

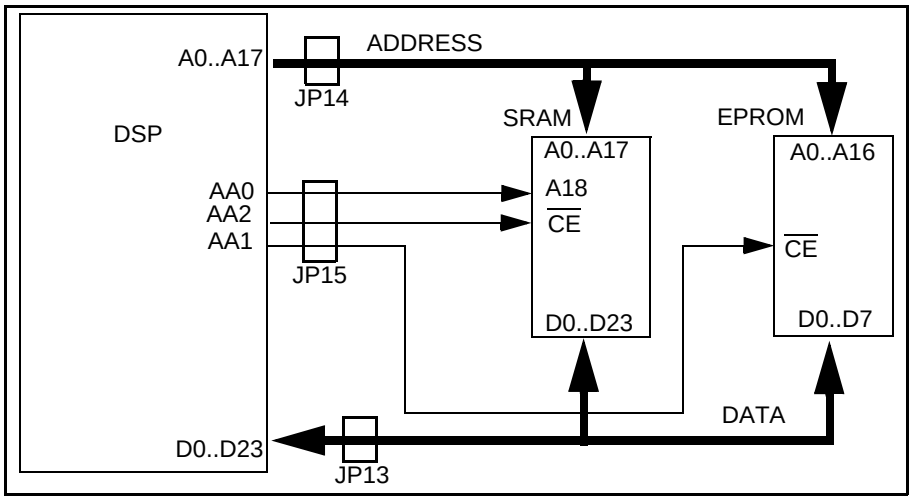

Figure 2-21 External Memory Interface Diagram

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2.11 POWER SUPPLY

The Evaluation Module requires an input voltage of 7.5-9V AC/DC (recommended 1A) for both analog and digital circuits. It has separate digital and analog power and ground planes and voltage regulators to output the +5V, +5VA and +3.3V supplies. The DC-DC converter outputs the -5V supply. When power is supplied to the 2.1mm power connector P2 or to the 2-pin terminal block P3, the green LED D8 is powered on. The polarity of the voltage applied to the P3 terminal block is reversible because the power goes through a bridge rectifier.

Note: While the voltage regulators can accommodate higher input voltage potentials, the added heat dissipation required at these input voltage levels results in the regulator becoming dangerously warm. It is recommended that users do not subject the board to power inputs in excess of the 12V.

2.11.1 POWER SUPPLY BLOCK DIAGRAM

The following figure shows the functional block diagram of the power supply circuit.

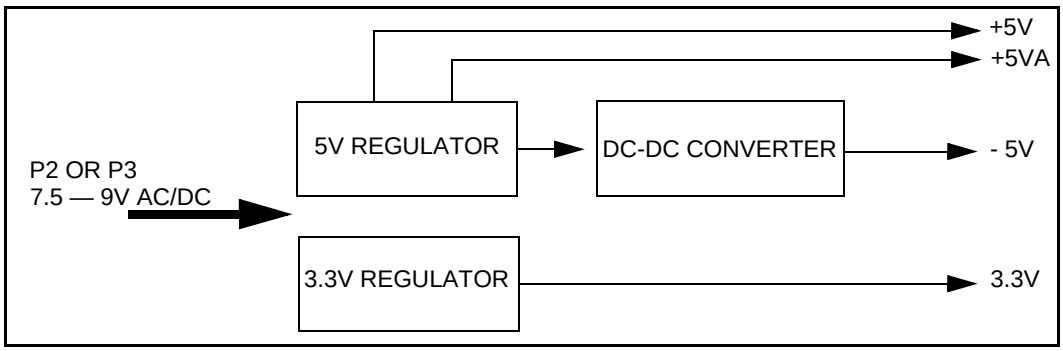

Figure 2-22 Evaluation Module Power Supply Diagram

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2.11.2 DSP POWER

For power consumption measurement, jumpers are available to connect the DSP's power pins to the power supply. Jumpers are placed in the headers shown in Table 2-19, the Evaluation Module supplies power to the DSP. Jumpers can be removed to provide access for power measurements.

Table 2-19 DSP Power Supply

JPx	POWER	DESCRIPTION
JP1	V_{CCC}	BUS CONTROL
JP2	V_{CCD}	DATA BUS
JP3	V_{CCH}	HOST
JP4	V_{CCA}	ADDRESS BUS
JP5	V_{CCS}	SHI, ESAI, DAX, TIMER
JP6	V_{CCQL}	QUIET CORE (LOW) POWER
JP7	V_{CCQH}	QUIET CORE (HIGH) POWER

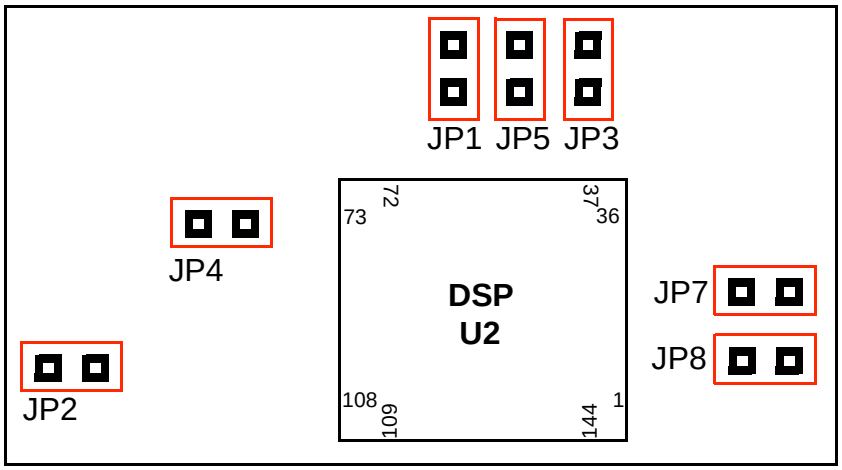

Figure 2-23 DSP Power Jumpers

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SECTION 3

COMPONENT DATASHEETS

3.1 DOCUMENTATION

Documentation for the audio components can be downloaded from the manufacturer websites shown in the following table. The Motorola web site for the appropriate manuals is:

http://www.mot.com/pub/SPS/DSP/LIBRARY/

Table 3-1 Documentation Location

Motorola Devices	DESCRIPTION	Motorola Document Order Number
DSP56362	Product Brief	DSP56362P/D
	Technical Datasheet	DSP56362/D
	User Manual	DSP56362UM/D
	Family Manual	DSP56300FM/D
Other Devices	**DESCRIPTION**	**LOCATION**
PCM1800	Technical Datasheet	http://www.burr-brown.com/download/DataSheets/PCM1800.pdf
PCM1716	Technical Datasheet	http://www.burr-brown.com/Products/DataSheets/PCM1716.pdf
CS8414	Technical Datasheet	http://www.cirrus.com/ftp/pubs/8413-4.pdf
CS8402	Technical Datasheet	http://www.cirrus.com/ftp/pubs/8401.pdf

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SECTION 4

SCHEMATICS

The schematics for the DSP56362EVM are included in the following pages. The bill of material is listed in Section 5.

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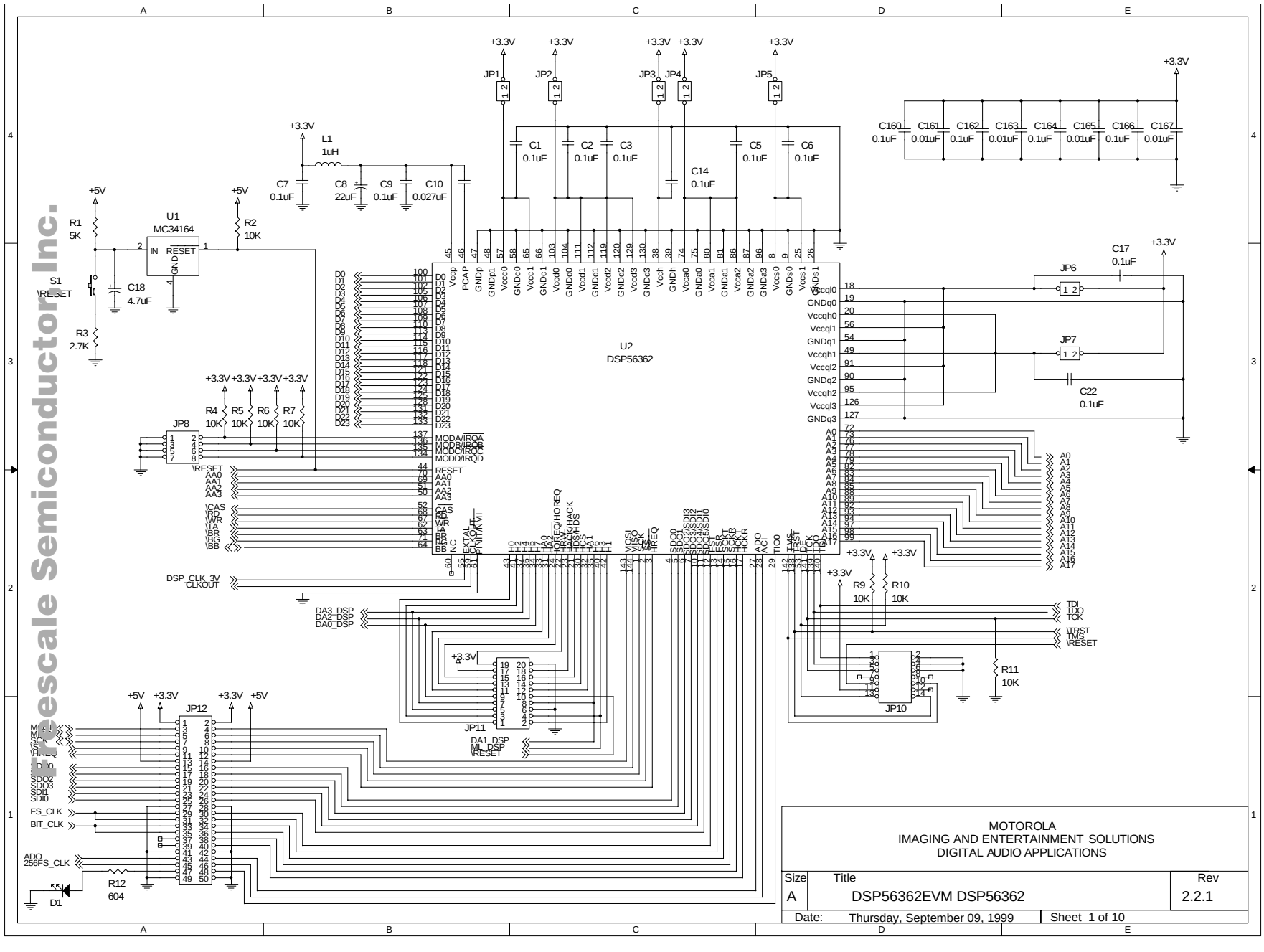
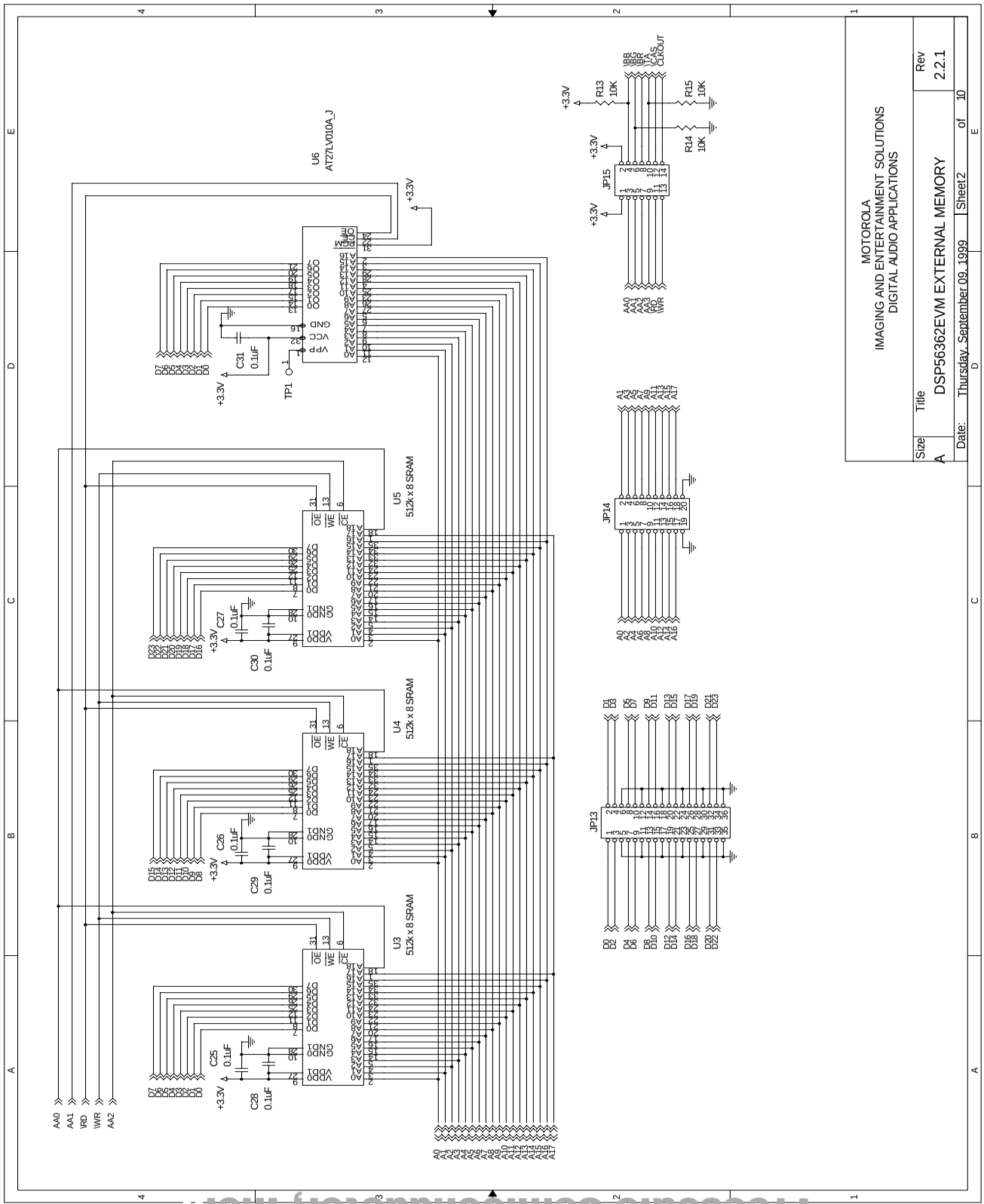
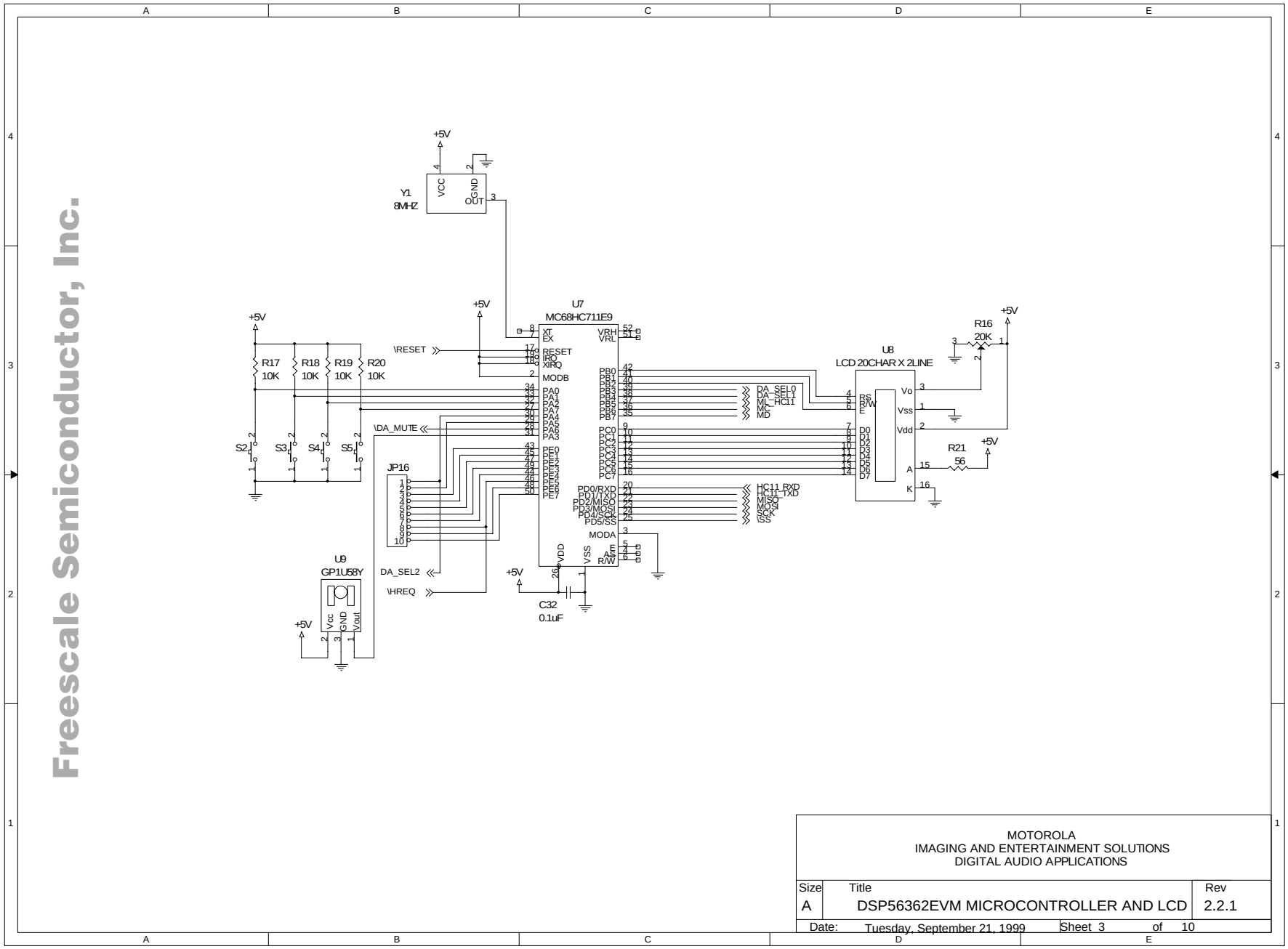
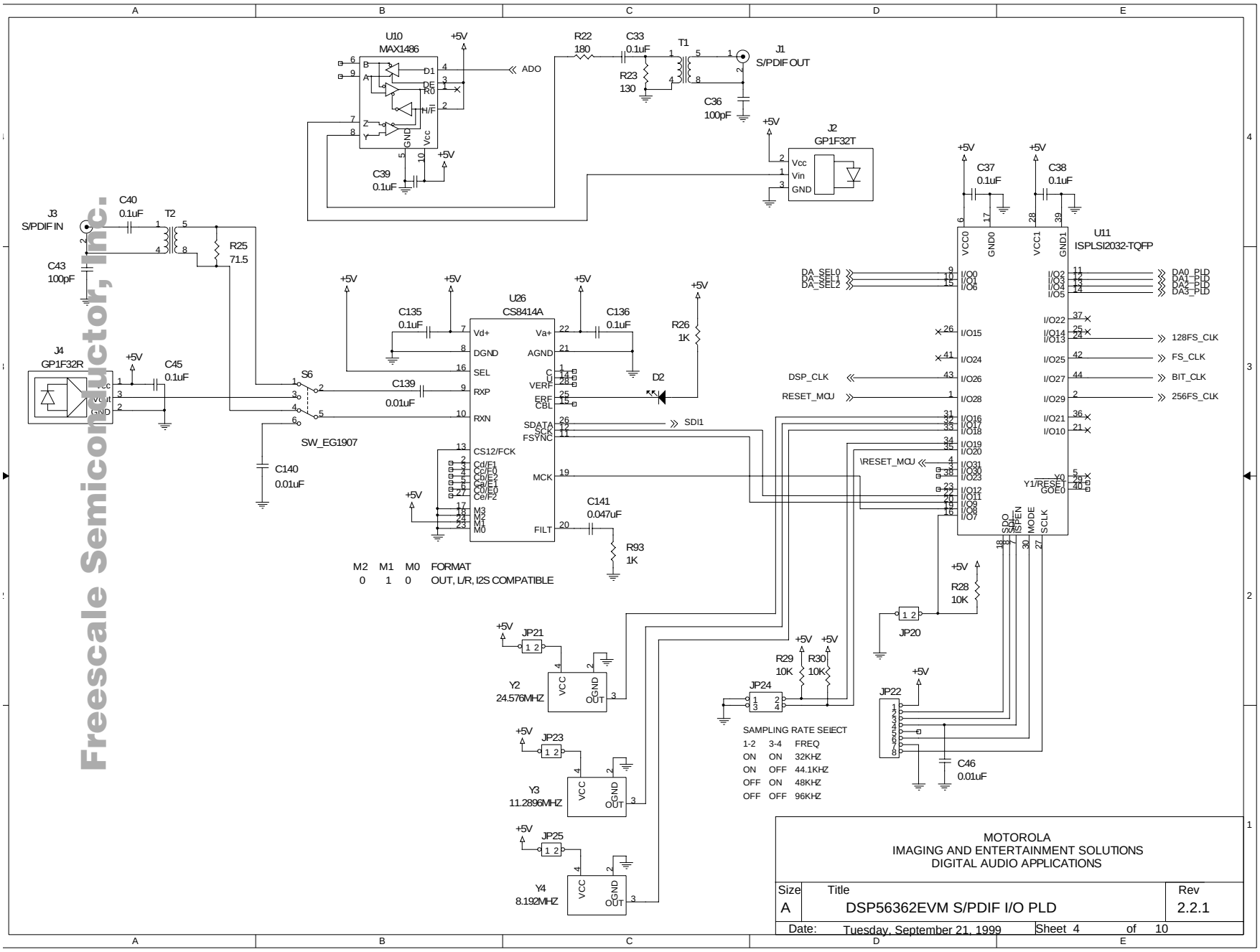

Freescale Semiconductor, Inc.
U1
MC34164
U2
DSP56362
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
JP10
JP11
JP12
L1
1uH
C1 0.1uF
C2 0.1uF
C3 0.1uF
C5 0.1uF
C6 0.1uF
C14 0.1uF
C7 0.1uF
C8 22uF
C9 0.1uF
C10 0.027uF
C160 0.1uF
C161 0.01uF
C162 0.1uF
C163 0.01uF
C164 0.1uF
C165 0.01uF
C166 0.1uF
C167 0.01uF
C17 0.1uF
C22 0.1uF
C18 4.7uF
R1 5K
R2 10K
R3 2.7K
R4 10K
R5 10K
R6 10K
R7 10K
R9 10K
R10 10K
R11 10K
R12 604
S1
\RESET
D1
+3.3V
+5V
DSP_CLK_3V
CLKOUT
DA3_DSP
DA2_DSP
DA0_DSP
DA1_DSP
ML_DSP
\RESET
FS_CLK
BIT_CLK
ADO
256FS_CLK
TDI
TDO
TCK
\TRST
TMS
\RESET
MOTOROLA
IMAGING AND ENTERTAINMENT SOLUTIONS
DIGITAL AUDIO APPLICATIONS
Size
A
Title
DSP56362EVM DSP56362
Rev
2.2.1
Date: Thursday, September 09, 1999
Sheet 1 of 10

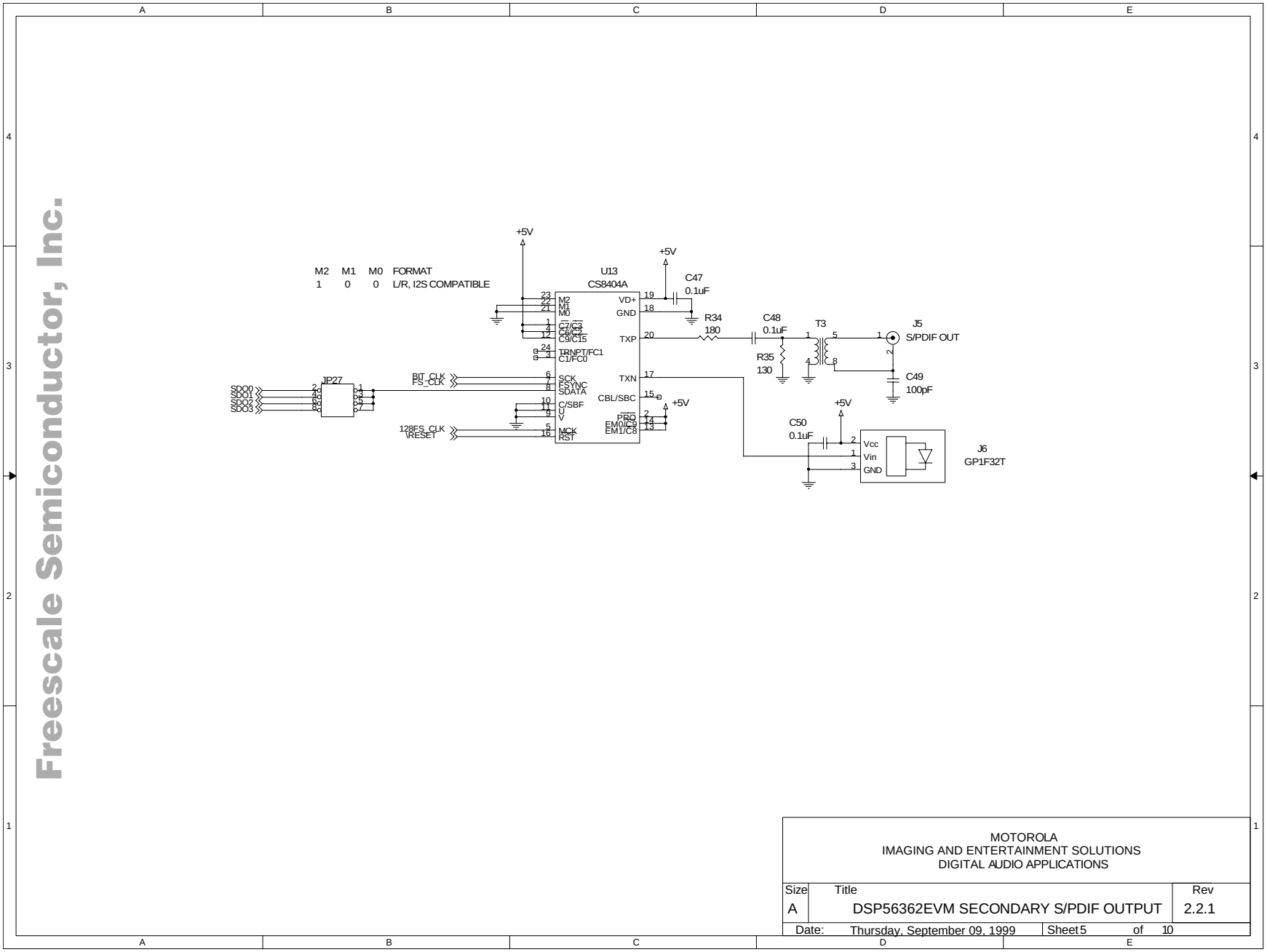


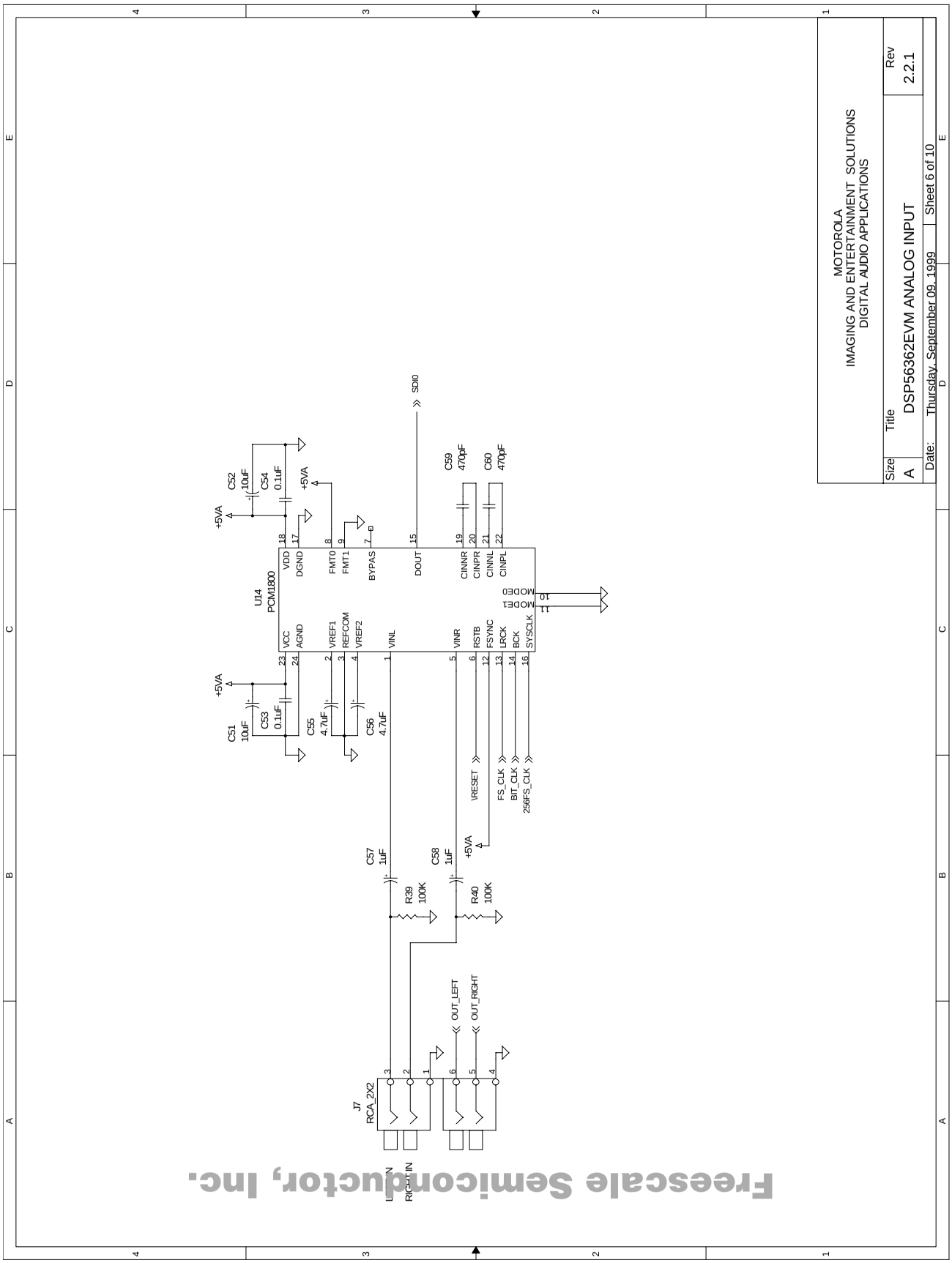
Freescale Semiconductor, Inc.


Freescale Semiconductor, Inc.
Y1
8MHZ
VCC
GND
OUT
+5V
U7
MC68HC711E9
XT
EX
VRH
VRL
RESET
IRQ
XIRQ
MODB
MODA
VDD
VSS
AS
E
R/W
PA0
PA1
PA2
PA7
PA4
PA5
PA6
PA3
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PD0/RXD
PD1/TXD
PD2/MISO
PD3/MOSI
PD4/SCK
PD5/SS
\RESET
\DA_MUTE
DA_SEL2
\HREQ
DA_SEL0
DA_SEL1
ML_HC11
MC
MD
HC11_RXD
HC11_TXD
MISO
MOSI
SCK
\SS
R17 10K
R18 10K
R19 10K
R20 10K
S2
S3
S4
S5
JP16
U9
GP1U58Y
Vcc
GND
Vout
C32
0.1uF
U8
LCD 20CHAR X 2LINE
RS
R/W
E
D0
D1
D2
D3
D4
D5
D6
D7
Vo
Vss
Vdd
A
K
R16
20K
R21
56
MOTOROLA
IMAGING AND ENTERTAINMENT SOLUTIONS
DIGITAL AUDIO APPLICATIONS
Size
A
Title
DSP56362EVM MICROCONTROLLER AND LCD
Rev
2.2.1
Date:
Tuesday, September 21, 1999
Sheet 3 of 10

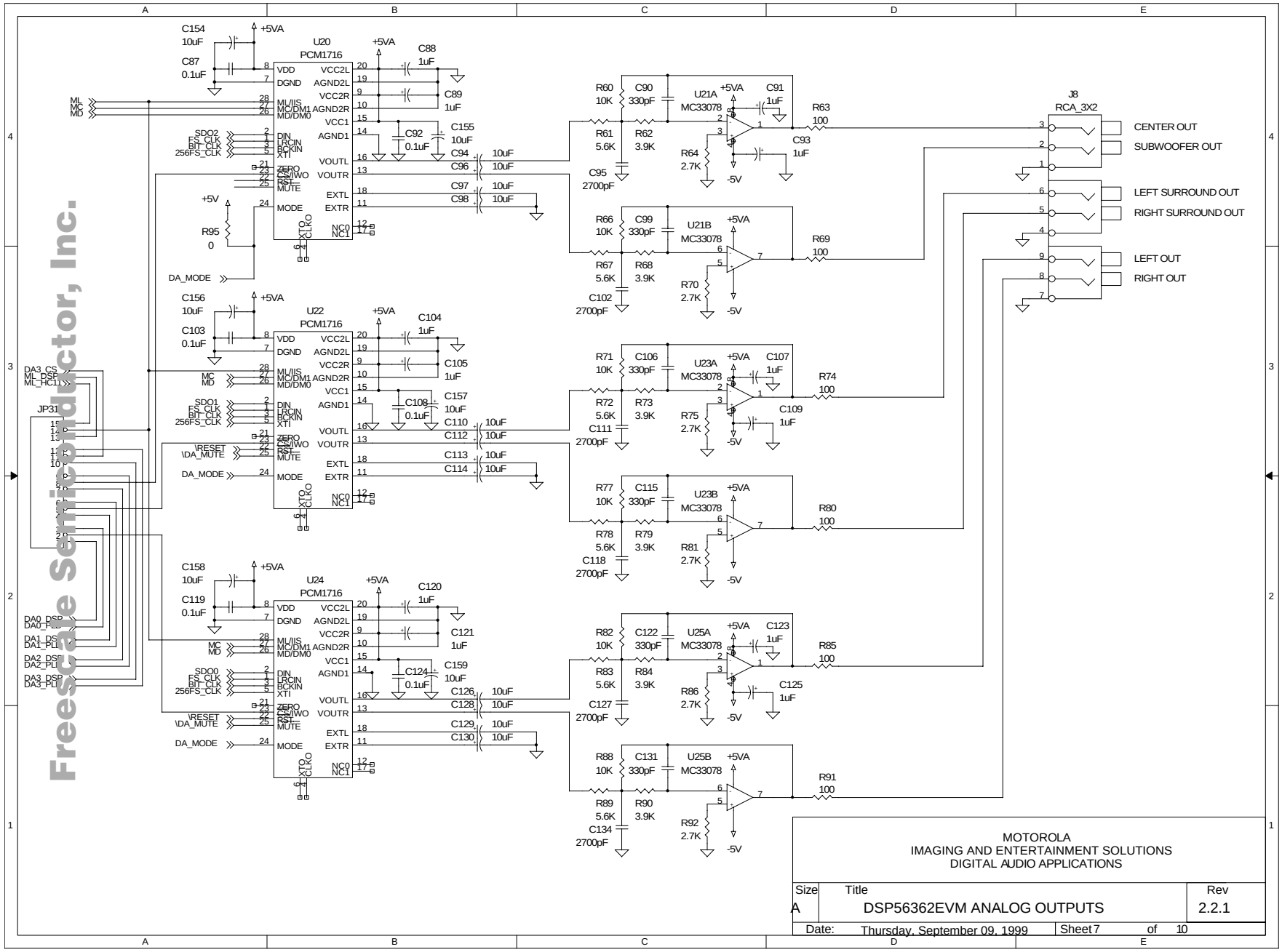


Freescale Semiconductor, Inc.

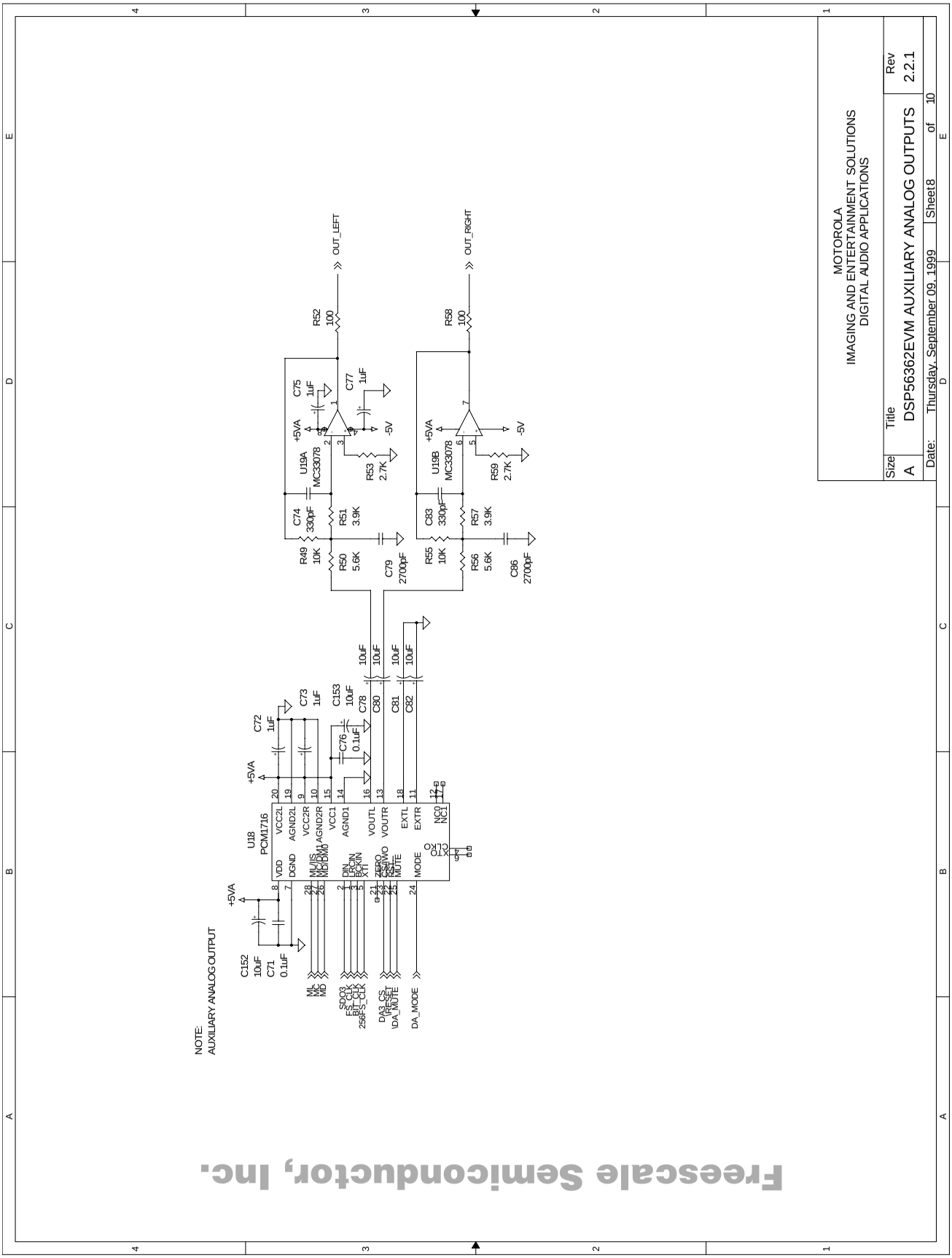

Freescale Semiconductor, Inc.
M2 M1 M0 FORMAT
1 0 0 L/R, I2S COMPATIBLE
+5V
U13
CS8404A
M2
M1
M0
C7/C3
C6/C2
C9/C15
TRNPT/FC1
C1/FC0
SCK
FSYNC
SDATA
C/SBF
U
V
MCK
RST
VD+
GND
TXP
TXN
CBL/SBC
PRO
EM0/C9
EM1/C8
C47
0.1uF
R34
180
C48
0.1uF
T3
J5
S/PDIF OUT
R35
130
C49
100pF
C50
0.1uF
Vcc
Vin
GND
J6
GP1F32T
JP27
SDO0
SDO1
SDO2
SDO3
BIT_CLK
FS_CLK
128FS_CLK
\RESET
MOTOROLA
IMAGING AND ENTERTAINMENT SOLUTIONS
DIGITAL AUDIO APPLICATIONS
Size
A
Title
DSP56362EVM SECONDARY S/PDIF OUTPUT
Rev
2.2.1
Date: Thursday, September 09, 1999
Sheet 5 of 10



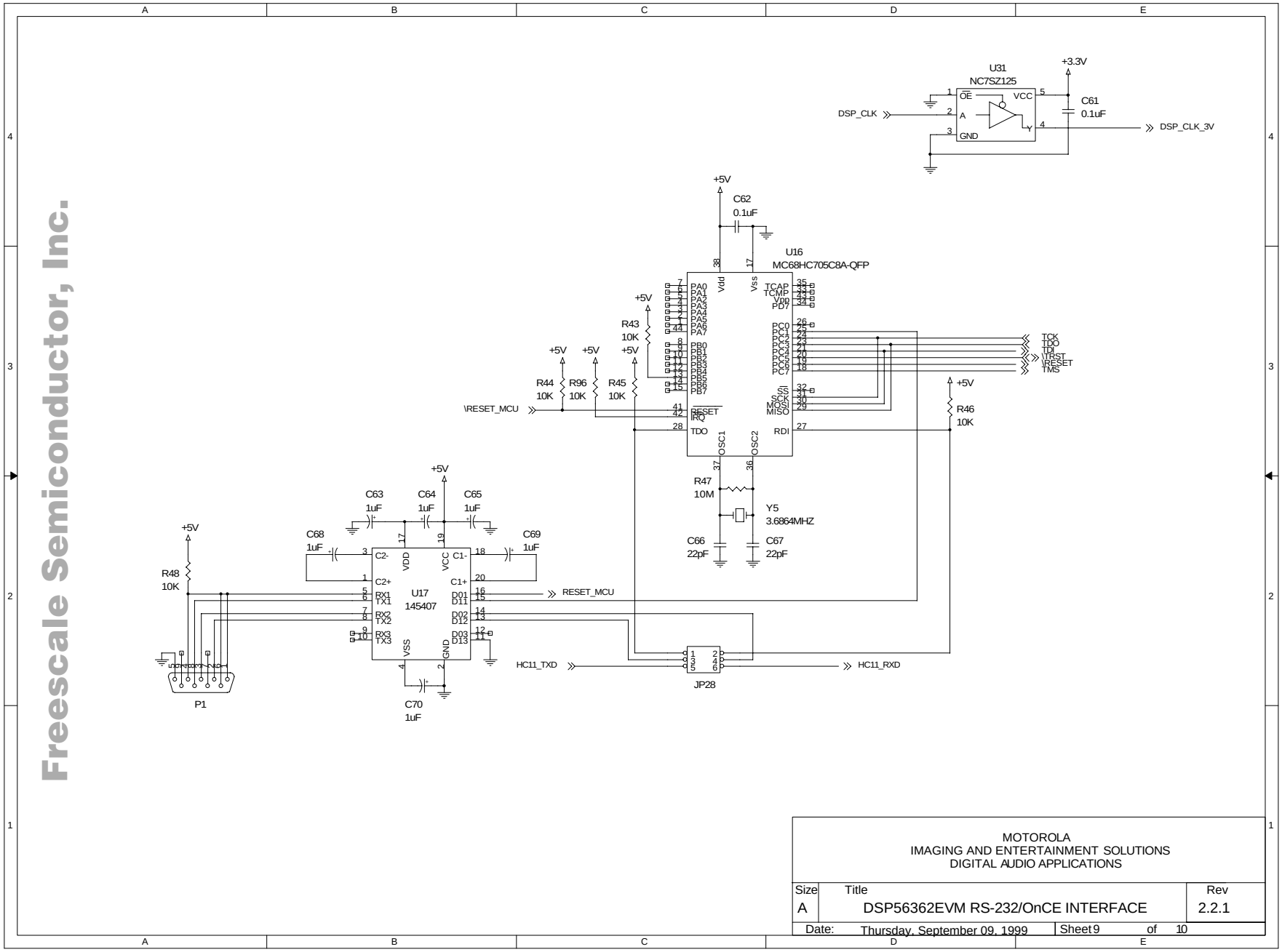
Freescale Semiconductor, Inc.



Freescale Semiconductor, Inc.



Freescale Semiconductor, Inc.


Freescale Semiconductor, Inc.
U31
NC7SZ125
OE
VCC
A
Y
GND
DSP_CLK
DSP_CLK_3V
C61
0.1uF
+3.3V
C62
0.1uF
U16
MC68HC705C8A-QFP
Vdd
Vss
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
TCAP
TCMP
Vpp
PD7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
SS
SCK
MOSI
MISO
RESET
IRQ
TDO
RDI
OSC1
OSC2
R43
10K
R44
10K
R96
10K
R45
10K
R46
10K
\RESET_MCU
TCK
TDO
TDI
\TRST
\RESET
TMS
R47
10M
Y5
3.6864MHZ
C66
22pF
C67
22pF
C63
1uF
C64
1uF
C65
1uF
C68
1uF
C69
1uF
C70
1uF
U17
145407
VDD
VCC
VSS
GND
C1+
C1-
C2+
C2-
RX1
TX1
RX2
TX2
RX3
TX3
D01
D11
D02
D12
D03
D13
R48
10K
P1
RESET_MCU
HC11_TXD
HC11_RXD
JP28
MOTOROLA
IMAGING AND ENTERTAINMENT SOLUTIONS
DIGITAL AUDIO APPLICATIONS
Size
A
Title
DSP56362EVM RS-232/OnCE INTERFACE
Rev
2.2.1
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Thursday, September 09, 1999
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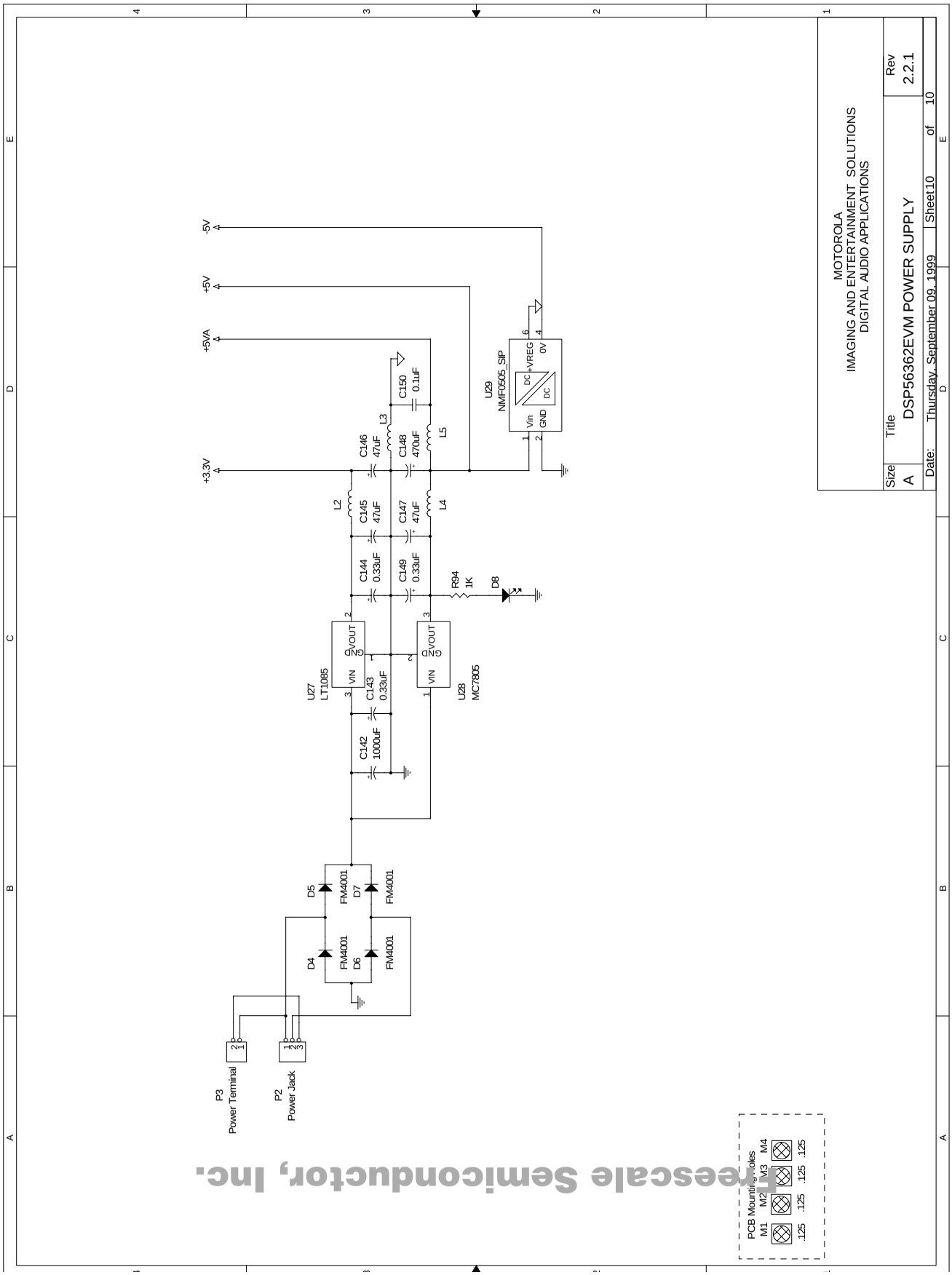

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SECTION 5

BILL OF MATERIALS

5.1 EVALUATION MODULE PARTS

The following table contains information on the parts and devices in the Evaluation Module. Contact information for suppliers of key devices is also included in Table 5-1.

Table 5-1 Evaluation Module Bill of Materials

Reference Designator	Description	Manufacturer	MFG P/N
C46, C139, C140, C161, C163, C165, C167	0.01uF, CHIPCAP 0805, 50V/10% TOL	PANASONIC	ECU-V1H103KBG
C1, C2, C3, C5, C6, C7, C9, C14, C17, C22, C25, C26, C27, C28, C29, C30, C31, C32, C33, C37, C38, C39, C40, C45, C47, C48,C50, C53, C54, C61, C62, C71,C76, C87, C92, C103, C108, C119, C124, C135, C136, C150, C160, C162, C164, C166	0.1uF, CHIPCAP 0805, 50V/20% TOL	AVX	08055E104MATMA
C8	22uF, TANTALUM ELECTROLYTIC SMD, 6.3V/EIA SIZE B	PANASONIC	ECS-T0JX226R
C10	0.027uF, CHIPCAP 0805, 50V/10% TOL	PANASONIC	ECU-V1H273KBX
C18, C55, C56	4.7uF, TANTALUM ELECTROL. SMD, 6.3V/EIA SIZE A	PANASONIC	ECS-T0JY475R
C36, C43, C49	100pF, CHIPCAP 0805, 50V/5% TOL	PANASONIC	ECU-V1H101JCG
C141	0.047uF, CHIPCAP 0805, 50V/10% TOL	XICON	CC501Z473M
C51, C52, C78, C80, C81, C82, C94, C96, C97, C98, C110, C112, C113, C114, C126, C128, C129, C130, C152, C153, C154, C155, C156, C157, C158, C159	10uF, TANTALUM ELECTROL. SMD, 6.3V/EIASIZE A	PANASONIC	ECS-T0JY106R
C57, C58, C63, C64, C65, C68, C69, C70, C72, C73, C75, C77, C88, C89, C91, C93, C104, C105,C107, C109, C120, C121, C123,C125	1uF, CHIPCAP 1206, 16V/20% TOL	PANASONIC	ECU-V1H471JCX
C59, C60	470pF, CHIPCAP 0805, 50V/5% TOL	PANASONIC	ECU-V1H471JCX
C66, C67	22pF, CHIPCAP 1206, 50V/5% TOL	PANASONIC	ECU-V1H220JCN

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Table 5-1 Evaluation Module Bill of Materials

Reference Designator	Description	Manufacturer	MFG P/N
C74, C83, C90, C99, C106, C115, C122, C131	330pF, CHIPCAP 0805, 50V/10% TOL	PANASONIC	ECU-V1H331KBN
C79, C86, C95, C102, C111, C118, C127, C134	2700pF, CHIPCAP 0805, 50V/10% TOL	PANASONIC	ECU-V1H272KBN
C148	470uF, RADIAL ALUMINUM ELECTROLYTIC, 10V	XICON	XRL10V470
C142	1000uF, MINI ALUM ELECTROL, 16V/AXIAL/0.394X0.984	XICON	XAH16V1000
C143, C144, C149	0.33uF. CHIPCAP 1206, 35V/20% TOL	PANASONIC	ECS-T1VY334R
C145, C146, C147	47uF, SUBMINI ALUM ELECROL, 10V/RADIAL/5X7	XICON	MLRL10V47
D1	YELLOW LED, SMD 1206	QT OPTOELECTRONICS	QTLP650D-3
D2	RED LED, SMD 1206	QT OPTOELECTRONICS	QTLP650C-2
D8	GREEN LED, SMD 1206	QT OPTOELECTRONICS	QTLP650C-4
D4, D5, D6, D7	RECTIFIER, 1.0 AMP SMD	RECTRON	FM4001
XXU8	DOUBLE ROW 16-PIN FEMALE HEADER, RECEPTACLE FOR U8	BERG	68683-608
JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP20, JP21, JP23, JP25	SINGLE ROW 2 PIN HEADER	BERG	86001-402
JP8, JP27	DOUBLE ROW 8 PIN HEADER	BERG	67997-408
JP10, JP15	DOUBLE ROW 14 PIN HEADER	BERG	67997-414
JP11, JP14	DOUBLE ROW 20 PIN HEADER	BERG	67997-420
JP12	DOUBLE ROW 50 PIN HEADER	BERG	67997-450
JP13	DOUBLE ROW 36 PIN HEADER	BERG	67997-436
JP16	SINGLE ROW 10 PIN HEADER	BERG	86001-410
JP35	Not Populated		
JP22	SINGLE ROW 8 PIN HEADER	BERG	86001-408
JP24	DOUBLE ROW 4 PIN HEADER	BERG	67997-404
JP28	DOUBLE ROW 6 PIN HEADER	BERG	67997-406

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Table 5-1 Evaluation Module Bill of Materials

Reference Designator	Description	Manufacturer	MFG P/N
JP31	TRIPLE ROW 15 PIN HEADER	BERG	68702-415
removed			
J1, J3, J5	RCA JACK	VIMEX	SCJ-0358B
J2, J6	OPTICAL TRANSMIT CONNECTOR	SHARP	GP1F32T
J4	OPTICAL RECEIVE CONNECTOR	SHARP	GP1F32R
J7	RCA JACK 2X2	VIMEX	JA0400721G
J8	RCA JACK 3X2	VIMEX	JA0600731G
L1	1uH INDUCTOR, SMD/2.5X3.2	TOKO	TKS1025CT
L2, L3, L4, L5	FERRITE BEAD	FUTURE	BL01RN1-A62
XU6	SOCKET FOR U6, 32P PIN PLCC/THRU HOLE	MOUSER	151-1033
XU7	SOCKET FOR U7, 52 PIN PLCC/THRU HOLE	MOUSER	151-1053
P1	DB9 CONNECTOR, RT ANGLE/PCB MOUNT	MOUSER	152-3409
P2	2.1MM POWER CONNECTOR	SWITCHCRAFT	93F7716
P3	2 PIN TERMINAL BLOCK	AUGAT	2SV-02
R1	5.1K, CHIP RES 0805, 1/10WATT 5%	PANASONIC	ERJ-6GEYJ512V
R2, R4, R5, R6, R7, R9, R10, R11, R13, R14, R15, R17, R18, R19, R20, R28, R29, R30, R43, R44, R45, R46, R48, R49, R55, R60, R66, R71, R77, R82, R88, R96	10K, CHIP RES 0805, 1/10WATT 5%	PANASONIC	ERJ-6GEYJ103V
R3, R53, R59, R64, R70, R75, R81, R86, R92	2.7K, CHIP RES 0805, 1/10WATT 5%	PANASONIC	ERJ-6GEYJ272V
R12	604, CHIP RES 0805,1/10WATT 1%	PANASONIC	ERJ-6ENF6040V
R22, R34	182, CHIP RES 0805,1/8WATT 1%	PANASONIC	ERJ-6ENF1820V
R23, R35	127, CHIP RES 0805, 1/8WATT 1%	PANASONIC	ERJ-6ENF1270V
R95	0, CHIP RES 0805, 1/10WATT 5%	PANASONIC	ERJ-6GEY0R00V
R25	71.5, CHIP RES 0805, 1/10WATT 1%	PANASONIC	ERJ-6ENF71R5V
R26, R93, R94	1K, CHIP RES 0805, 1/10WATT 5%	PANASONIC	ERJ-6GEYJ102V
R39, R40	100K, CHIP RES 0805, 1/10WATT 5%	PANASONIC	ERJ-6GEYJ104V

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Table 5-1 Evaluation Module Bill of Materials

Reference Designator	Description	Manufacturer	MFG P/N
R50, R56, R61, R67, R72, R78, R83, R89	5.62K, CHIP RES 0805, 1/10WATT 1%	PANASONIC	PERJ-6ENF5621V
R51, R57, R62, R68, R73, R79, R84, R90	3.92K, CHIP RES 0805, 1/10WATT 1%	PANASONIC	ERJ-6ENF3921V
R52, R58, R63, R69, R74, R80, R85, R91	100, CHIP RES 0805, 1/10WATT 1%	PANASONIC	ERJ-6ENF101V
R47	10M, CHIP RES 0805, 1/10WATT 5%	PANASONIC	ERJ-6GEYJ106V
R21	56, CHIP RES 0805, 1/10WATT 5%	PANASONIC	ERJ-6GEYJ560V
S6	SLIDE SWITCH DPDT	E-SWITCH	EG2209
S1, S2, S3, S4, S5	6MM PUSHBUTTON SWITCH	PANASONIC	EVQ-QS205K
R16	TRIMPOT 20K	PANASONIC	EVN-D8AA03B24
T1, T2, T3	96KHZ DIGITAL TRANSFORMER	SCIENTIFIC CONVERSION	SC979-03
U1	UNDERVOLTAGE SENSOR	MOTOROLA	MC34164D-5
U2	DSP, 144PIN/TQFP *please see note #68	MOTOROLA	DSP56362
U3, U4, U5	128KX8 SRAM, 3.3V/400MIL	GSI TECHNOLOGY	GS71108J-10
U6	128KX8 EPROM, 3.3V/32 PIN PLCC, *please see note #70	ATMEL	AT27LV010A-15JC
U7	8-BIT MICROCONTROLLER, 52 PIN PLCC *please see note #71	MOTOROLA	MC68HC711E20VFN2
U8	LCD 20CHAR X 2LINE	POWERTIP	PC2002LRU-AEA-B
U9	Not Populated		
U10	MAX1486	MAXIM	MAX1486CUB
U11	PLD (See PLD Equations following this BOM)	LATTICE	ISPLSI2032-110LT44
U12	Not populated		
U13	DIGITAL AUDIO TRANSMITTER	CRYSTAL	CS8404A-CS
U14	20-BIT A/D CONVERTER, 24-PIN/SSOP	BURR-BROWN	PCM1800
U31	BUFFER WITH 3 STATE OUTPUT, SOT23-5	FAIRCHILD	NC7SZ125M5
U16	8-BIT MICROCONTROLLER	MOTOROLA	MC68HC705C8ACFB
U17	RS-232 TRANSCEIVER	MOTOROLA	MC145407DW

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Table 5-1 Evaluation Module Bill of Materials

Reference Designator	Description	Manufacturer	MFG P/N
U18, U20, U22, U24	DELTA-SIGMA D/A CONVERTER	BURR-BROWN	PCM1716
U19, U21, U23, U25	OP-AMP, SO-8	BURR-BROWN	BBOPA2134UA
U26	DIGITAL AUDIO RECEIVER	CRYSTAL	CS8414-CS
U27	3.3V REGULATOR, TO-220	LINEAR TECH.	LT1085CT-3.3
U28	5V REGULATOR, TO-220	MOTOROLA	MC7805ACT
U29	DC-DC CONVERTER	NEWPORT TECH.	NMF0505S
U30	Not Populated		
Y1	8MHZ OSCILLATOR, SMD	MMD	MI5050H-8MHZ
Y2	24.576MHZ OSCILLATOR, SMD	MMD	MI5050H-24.576MHZ
Y3	11.2896MHZ OSCILLATOR, SMD	MMD	MI5050H-11.2896MHZ
Y4	8.192MHZ OSCILLATOR, SMD	MMD	MI5050H-8.192MHZ
Y5	3.6864MHZ CRYSTAL, HC49	ECS	X403
Mounting hardware for ‘U8’ and standoffs for the four corners of the PC board.	Standoffs	H.H. Smith	30F1463
Mounting hardware for ‘U8’ and standoffs for the four corners of the PC board.	Screws	Waldom	FN-817-C
XU28	Heatsink for U28 T0-220, L=0.75, W=0.520, H=0.500 (above dimensions are in inches)	AAVID Thermal Technologies Inc.	577202B00000
XU8	DOUBLE ROW 16-PIN MALE HEADER MOUNTS TO BOTTOM SIDE OF U8 LCD	BERG	68683-608
SHUNTS	SHUNT CONN., 2 POSITION	3M	929955-06
Note #68. This part is mounted on a socket and the part information for the socket is given in the following columns	Yamaichi 144 pin TQFP socket	Yamaichi Electronics	IC149-144-045-S5
Note #70. This part is mounted on a socket and the part information for the socket is given in the following columns	Mouser PLCC socket, 32 pin	Mouser	151-1533
Note #71. This part is mounted on a socket and the part information for the socket is given in the following columns. The programmed part in installed in the socket.	Mouser PLCC socket, 52 pin	Mouser	151-1553

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5.2 PLD EQUATIONS

```
Declarations

"inputs
SEL1..SEL0          pin 34,35;
CLK8M               pin 33;
CLK11M              pin 32;
CLK24M              pin 31;
CS_LRCK             pin 20; "FS CLOCK from the CS8414
CS_SCK              pin 22; "BIT CLOCK from the CS8414
RESET_MCU           pin 1;
DA_SEL1..DA_SEL0    pin 10,9;
DA_SEL2             pin 15;
CS_MCK              pin 19; "256 clock from the Crystal clock chip
JUMP                pin 16; "Jumper selection ON=AD : OFF=SPDiA


"outputs
FS_CLK              pin 42 istype 'com';
BIT_CLK             pin 44 istype 'com';
RESET_MCU_          pin 4; " Pin 5 in hardware but this pin can not be used.Oin 4 is
used instead.
FS_CLK256           pin 2 istype 'com'; "sync buffered version
FS_CLK128           pin 24 istype 'com';
DA3_PLD             pin 14;
DA2_PLD             pin 13;
DA1_PLD             pin 12;
DA0_PLD             pin 11;
DSP_CLK             pin 43; "output clk8m divided by 8 (dsp_clk)


"nodes
CLK12M              node istype 'reg_d';
div3..div0          node istype 'reg_d';
FM_CLK256           node istype 'com,keep,retain';
scale7..scale0      node istype 'reg_d';
DIV4                node;
DIV64               node;
DIV256              node;
FM_CLK256B          node istype 'keep,retain';


"sets
DIVIDE = [div3..div0];
FS_GEN = [scale7..scale0];


"constants
h,l,x,z,c  = 1,0,.x.,.z.,.c.;
```

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```
"plsi properties

plsi property 'Y1_AS_RESET OFF';
plsi property 'ENP FS_CLK128 npath1';
plsi property 'PRESERVE FM_CLK256';
plsi property 'PRESERVE FM_CLK256B';


Equations"
Internal Generation of FS/Bit clock when NO SPDiA is available
FS_GEN := FS_GEN + 1;
FS_GEN.CLK = !FM_CLK256B;


DIV256=scale7;
DIV64 = scale5;
DIV4 = scale1;


" Sync buffered version of FS clock
FS_CLK = (JUMP & DIV256) # (!JUMP & CS_LRCK);


" Sync buffered version of BIT clock
BIT_CLK = (JUMP & DIV4) # (!JUMP & CS_SCK);


" Buffered reset signals
RESET_MCU_ = !RESET_MCU;

"Multiplexed clock outputs : drives fs_CLK256 when Crystal not SELected
FM_CLK256 = ((!SEL1 & !SEL0 & CLK8M)
           # (!SEL1 &  SEL0 & CLK11M)
           # ( SEL1 & !SEL0 & CLK12M)
           # ( SEL1 &  SEL0 & CLK24M));

FM_CLK256B = ((!SEL1 & !SEL0 & CLK8M)
            # (!SEL1 &  SEL0 & CLK11M)
            # ( SEL1 & !SEL0 & CLK12M)
            # ( SEL1 &  SEL0 & CLK24M));

" SDF Rcvr PLL input to the 256/128 outputs

FS_CLK256 = (JUMP & FM_CLK256) # (!JUMP & CS_MCK);

FS_CLK128 = ( FS_CLK128 $ ((JUMP & FM_CLK256 & !FS_CLK256) # (!JUMP &CS_MCK &
!FS_CLK256)));

" Divide by 2 for the Clock input Mux

CLK12M := !CLK12M;
CLK12M.CLK = CLK24M;
```


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PLD Equations

```
"Divide by 8 for the 8 Mhz Clock input with direct output path

DIVIDE := DIVIDE + 1;
DIVIDE.CLK = CLK8M;

//DSP_CLK = div3;
DSP_CLK = CLK8M;

//XTI = FM_CLK256 & !JUMP;     "If no jumper at J20 and DIR is on thenY2-Y4
                               "are used to generate the all the bit clocks
                               "for the AD converters.
// XTI is not used in the rev 2.2 of the EVM - Mithra 08/24/99


" 2 to 4 Decoder
!DA3_PLD = ((!DA_SEL2 & DA_SEL1  &  DA_SEL0) # (DA_SEL2 & !DA_SEL1 &!DA_SEL0));
!DA2_PLD = ((!DA_SEL2 & DA_SEL1  & !DA_SEL0) # (DA_SEL2 & !DA_SEL1 &!DA_SEL0));
!DA1_PLD = ((!DA_SEL2 & !DA_SEL1 &  DA_SEL0) # (DA_SEL2 & !DA_SEL1 &!DA_SEL0));
!DA0_PLD = ((!DA_SEL2 & !DA_SEL1 & !DA_SEL0) # (DA_SEL2 & !DA_SEL1 &!DA_SEL0));


END
```

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SECTION 6

RUNNING THE PASS-THROUGH CODE

The Evaluation Module includes an HC11 with the pass-through files programmed in the EPROM. The pass-through software allows users to input and output audio to the Evaluation Module without loading the files through the OnCE (stand-alone mode).

6.1 PASS-THROUGH OPERATION

The main loop of the `digital.asm` and `analog.asm` programs serve as a reference guide on how to pass data into and out of the EVM.

6.1.1 RECEIVE INTERRUPT SERVICE ROUTINES

The receive interrupt service routine esai_rx_isr moves the left data word from the receive data register RXn (RX0 or RX1) into the receive left data buffer RX_BUFF_BASE and moves the right data word from the receive data register RXn into the receive right data buffer RX_BUFF_BASE+1. The pointer to the RX_BUFF_BASE has modulo of 2, so it alternates between the left and right receive buffers.

If the serial receive shift register SDI0 or SDI1 is filled and ready to transfer to the receiver data register RXn and RXn is already filled, then the Receiver Overrun Error Flag (ROE) is set and the receive with exception interrupt service routine esai_rxe_isr is called. This routine clears the ROE bit.

The receive last slot interrupt service routine `esai_rxls_isr` resets the buffer pointer to RX_BUFF_BASE in case the pointer is corrupted after the last slot of the frame. For example, after the right data is received.

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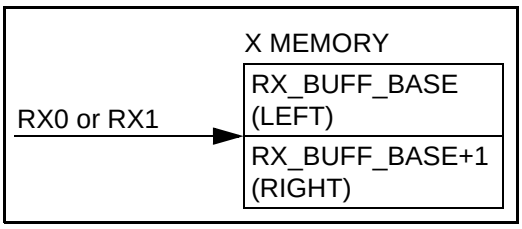

Figure 6-1 Receive Input Buffer

```
          esai_rxe_isr          ; ESAI RECEIVE WITH EXCEPTION ISR
          bclr      #7,x:M_SAISR; Read SAISR to clear receive
                                ; overrun error flag

          esai_rx_isr           ; ESAI RECEIVE ISR
                    move    r0,x:(r6)+ ; Save r0 to the stack
                    move    m0,x:(r6)+ ; Save m0 to the stack
                    move    #1,m0 ; Modulus 2 buffer
                    move    x:RX_PTR,r0 ; Load the pointer to the rx buffer
                    nop
                    jset#$6,x:M_SAISR,LeftSlot
                    bset#RightReceive,x:flags
                    movep   x:M_RX1,x:(r0)+; Receive from RX1 in this case
                    move    r0,X:RX_PTR
                    move    x:-(r6),m0 ; Restore m0
                    move    x:-(r6),r0 ; Restore r0
                    rti

esai_rxls_isr                   ; ESAI RECEIVE LAST SLOT ISR
                    move    r0,x:(r6)+ ; Save r0 to the stack
                    move    #RX_BUFF_BASE,r0; Reset rx buffer pointer just in
                                      ; case it was corrupted
                    move    r0,x:RX_PTR ; Update rx buffer pointer
                    move    x:-(r6),r0 ; Restore r0rti
```

Figure 6-2 Receive Interrupt Service Routines

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6.1.2 TRANSMIT INTERRUPT SERVICE ROUTINES

The transmit interrupt service routine moves the left data word from the transmit left data buffer TX_BUFF_BASEinto the transmit data register TXn (TX0, TX1, TX2 or TX3) and moves the right data word from the transmit right data buffer TX_BUFF_BASE+1 into the transmit data register TXn. The pointer to the TX_BUFF_BASE has modulo of 2 so it alternates between left and right transmit buffers.

If the serial receive shift register SDI0 or SDI1 is filled and ready to transfer to the receiver data register RXn and RXn is already filled, then the Receiver Overrun Error Flag (ROE) is set and the receive with exception interrupt service routine esai_rxe_isr is called. This routine clears the ROE bit.

The receive last slot interrupt service routine esai_rxls_isr resets the buffer pointer to RX_BUFF_BASE in case the pointer is corrupted after the last slot of the frame. For example, after the right data is received.

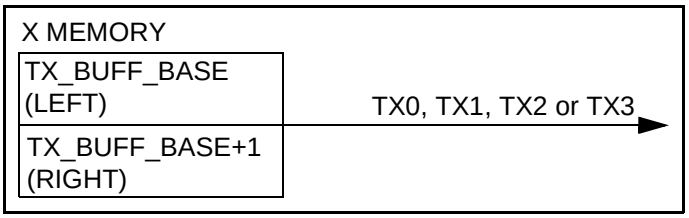

Figure 6-3 Transmit Output Buffer

```
esai_txe_isr          ; ESAI TRANSMIT WITH EXCEPTION ISR
          bclr        #14,x:M_SAISR ; Read SAISR to clear transmit;
                      underrun error flag

esai_tx_isr           ; ESAI TRANSMIT ISR
          mover0,x:(r6)+ ; Save r0 to the stack
          movem0,x:(r6)+ ; Save m0 to the stack
          move #1,m0 ; Modulus 2 buffer
          movex:TX_PTR,r0 ; Load the pointer to the Tx buffer
          nop

          movep       x:(r0),x:M_TX0; Transmit to TX0 in this case
          movep       x:(r0),x:M_TX1
          movep       x:(r0),x:M_TX2
          movep       x:(r0)+,x:M_TX3
          move        r0,x:TX_PTR ; Update tx buffer pointer
          move        x:-(r6),m0 ; Restore m0
          move        x:-(r6),r0 ; Restore r0rti

esai_txls_isr                  ; ESAI TRANSMIT LAST SLOT ISR
```


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```
move      r0,x:(r6)+ ; Save r0 to the stack
move      #TX_BUFF_BASE,r0 ; Reset pointer
move      r0,x:TX_PTR ; Reset tx buffer pointer just in
          ; case it was corrupted
move      x:-(r6),r0rti
```

Figure 6-4 Transmit Interrupt Service Routines

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6.1.3 MAIN LOOP

Bit 6 of the ESAI Status Register (SAISR) which is the receive frame sync flag (RFS) is polled to wait for a frame sync to occur. When the frame sync occurs, the contents of the input buffers RX_BUFF_BASE and RX_BUFF_BASE+1 are copied to accumulators a and b. Users can insert additional processing code at this point. If no processing is required, the contents of accumulators a and b are copied to the output buffers TX_BUFF_BASE and TX_BUFF_BASE+1. The program jumps back to the beginning of the loop for the next sample.

```
LOOP
          jclr #RightRecieve,X:flags,*
          bclr #RightRecieve,X:flags
          move x:RX_BUFF_BASE,a ;receive left
          move x:RX_BUFF_BASE+1,b ;receive right
          move a,x:TX_BUFF_BASE ;transmit left
          move b,x:TX_BUFF_BASE+1 ;transmit right
          jmp LOOP
```

Figure 6-5 Passthrough Main Loop

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6.2 DIGITAL PASS-THROUGH

To use digital input, perform the following tasks:

1. Apply power to the Evaluation Module as shown in Installation Procedures, Section 1-5.
2. Connect the input and output audio cables.
3. Configure the jumpers as shown in the following table:

Table 6-1 Digital Input

Input Type	Input Connector	Output Connector	S6	JP20
Electrical	J3	J8	ELC	1-2
Optical	J4	J8	OPT	1-2

4. Press the reset switch S1.

The following screen appears on the LCD:

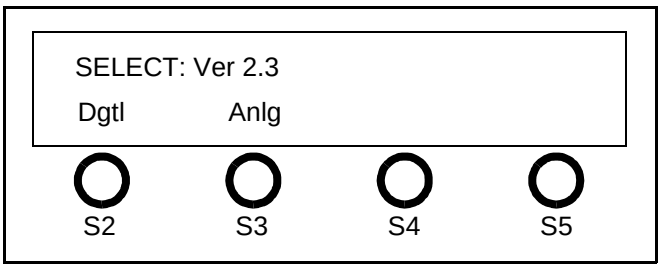

Figure 6-6 LCD Pass-through Screen

5. Press switch S2 and select digital input. Pass-through code downloads for approximately two seconds before audio output is heard.

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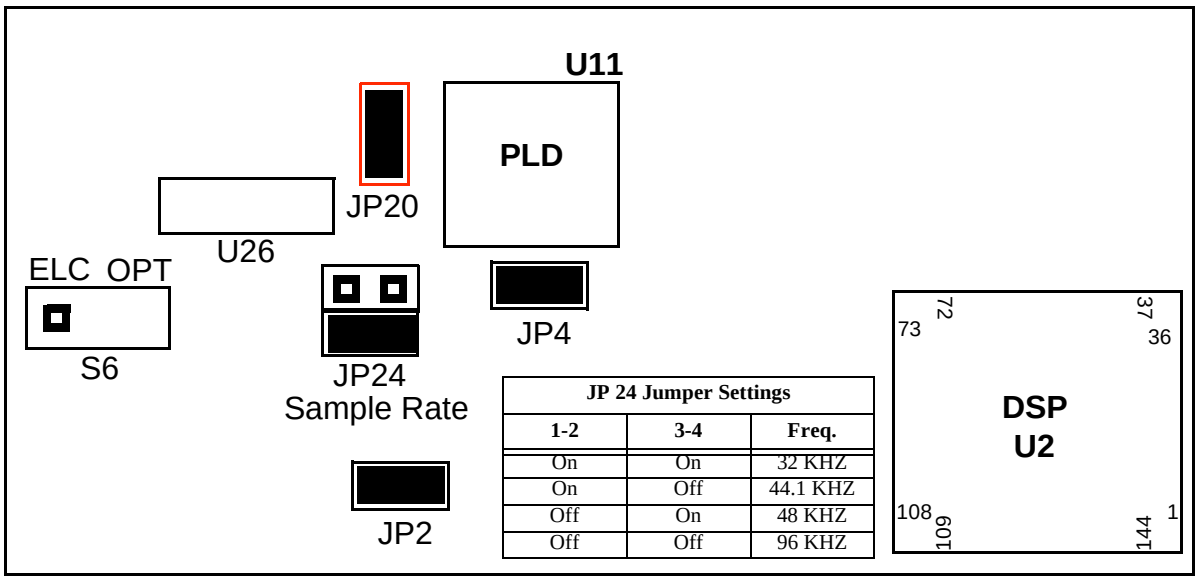
6.3 DIGITAL PASS-THROUGH JUMPER SETTINGS

The following figure shows the jumper settings when using the optical connector. Notice that JP20 is in and S6 must be set for the appropriate connector (optical or coax).



JP 24 Jumper Settings		
1-2	3-4	Freq.
On	On	32 KHZ
On	Off	44.1 KHZ
Off	On	48 KHZ
Off	Off	96 KHZ

Figure 6-7 Jumper Settings for Digital Pass-Through

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6.4 ANALOG PASS-THROUGH

To use analog input, perform the following tasks:

1. Apply power to the Evaluation Module as described in 1.4 Installation Procedures.
2. Connect the input and output audio cables.
3. Configure the jumpers as shown in the following table:

Table 6-2 Analog Input

Input Type	Input Connector	Output Connector	JP20
Analog	J7 Pins 2 and 3	J8	No Jumper

4. Press RESET switch S1. The following screen appears on the LCD:

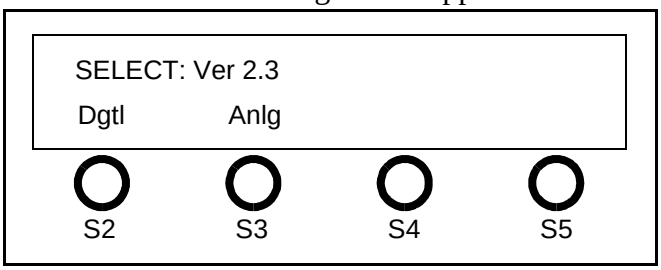

Figure 6-8 LCD pass-through Screen

5. Press switch S3 to select analog input. Pass-through code downloads for approximately two seconds before audio output is heard.

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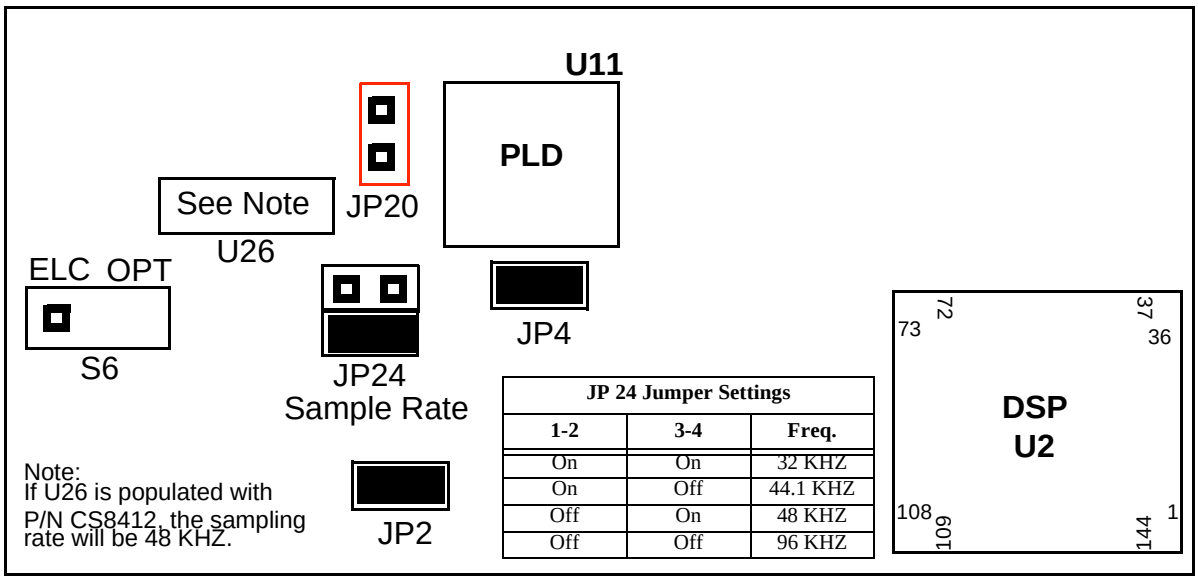
6.5 ANALOG PASS-THROUGH JUMPER SETTINGS

The following figure shows the jumper settings when using analog inputs. Notice that JP20 is removed and JP24 must be set according to the sampling rate.



JP 24 Jumper Settings		
1-2	3-4	Freq.
On	On	32 KHZ
On	Off	44.1 KHZ
Off	On	48 KHZ
Off	Off	96 KHZ

Figure 6-9 Jumper Settings for Analog Pass-Through

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Analog Pass-Through Jumper Settings

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